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The capabilities of a Swept Line Electron Beam (SLEB) in annealing ionimplanted semiconductors are examined. This technique employs a fixed geometry, line-shaped electron beam through which implanted samples are mechanically scanned. In general, this technique can produce annealing results comparable or superior to those achievable by conventional furnace annealing.

Residual point defects in self-implanted amorphous silicon treated by SLEB and furnace processes are examined by Deep Level Transient Spectroscopy.

20. Despite high temperature treatment, furnace annealed samples show large $(10^{16}~{\rm cm}^{-3})$ defect concentrations and dopant migration phenomena. This is especially true in the as-implanted amorphous-cyrstalline transition region. When proper annealing parameters are used, SLEB annealed material shows much reduced point defect concentrations and reduced dopant motion. These relatively thick amorphous layers $(0.5~\mu\text{m})$ are regrown and annealed by SLEB without the use of additional furance treatment.

Similar studies of BF2 implanted silicon are also presented. Differential resistivity/Hall effect and Secondary Ion Mass Spectrometry analysis are used to show improved electrical activation and only limited dopant motion during SLEB annealing as compared with furnace annealing. The improved electrical activity is especially significant in the original amorphous-crystalline transition region where reduced residual defect densities are observed.

SLEB annealing effectiveness in both direct and indirect band gap composition $GaAs_{1-x}P_x$ is also investigated. Photoluminescence emission from nitrogen implanted, beam annealed material is found to be comparable or larger in intensity when compared with optimally prepared furnace annealed material. Photoluminescence profiling and p-n junction studies show that migration of implanted nitrogen and related damage can be limited to the as-implanted profile when SLEB annealing is used.

SWEPT LINE ELECTRON BEAM ANNEALING OF ION-IMPLANTED SEMICONDUCTORS

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Kenneth James Soda

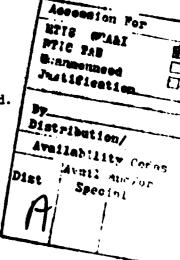
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SWEPT LINE ELECTRON BEAM ANNEALING OF ION-IMPLANTED SEMICONDUCTORS

BY

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THESIS

37.3

Submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering in the Graduate College of the University of Illinois at Urbana-Champaign, 1982

Urbana, Illinois

SWEPT LINE ELECTRON BEAM ANNEALING OF ION-IMPLANTED SEMICONDUCTORS

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Coordinated Science Laboratory and
Department of Electrical Engineering
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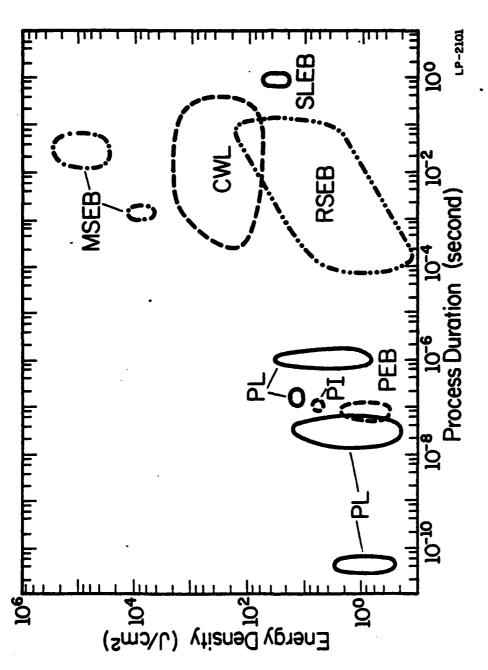
1. INTRODUCTION

1.1 Overview of Beam Processing Technology

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The use of concentrated beams of photons, electrons or ions to prepare semiconductor material has recently become an area of intense research. Although lasers have provided other industrial applications for many years, beam techniques have only recently demonstrated the potential to revolutionize semiconductor device fabrication. In this section, I outline recent developments and applications of beam processing, point out major trends and describe the relationship of my research to the mainstream of technology.

The techniques used for beam processing are distinguished by their beam source and method by which the beam energy is directed onto the semiconductor. To date, six beam processing techniques have been studied. These employ pulsed lasers (PL), raster scanned CW lasers (CWL), pulsed ion beams (PI), area pulsed electron beams (PEB), raster scanned (RSEB) or multiscanned electron beams (MSEB), and swept line electron beams (SLEB). A general overview of experimental processing parameters is presented in Figure 1.1. Here total average incident energy density is plotted against process duration. In cases of multiple scanning, energy density is summed after many passes by the beam. Data here are by no means all inclusive, but reflect the general range of each processing technique. Several trends are noteworthy. First, there is a tremendous span over which successful beam processing applications have occured; eleven orders of magnitude in time, seven orders in energy density. Much of the initial experimentation has concentrated on pulsed techniques, particularly pulsed lasers and the SPIRE area PEB machine. (See lower left of Figure 1.1.) Processing is generally



Representative energy density versus process duration parameters for the six major These techniques use: PL - Pulsed Lasers; Note the eleven order of magnitude range in process duration and PEB - Pulsed Electron Beams; PI - Pulsed Ion Beams; MSEB/RSEB - Multi or Raster Scanned Blectron Beams; CML - Continuous Wave Lasers; and SLEB - Swept-Line seven order of magnitude range in energy density. types of semiconductor beam processing. Electron Beams. F1g. 1.1.

performed in a single pulse, thus limiting experimental parameters to the characteristic laser or electron discharge decay. In more recent studies, scanned continuous lasers and electron beams (MSEL, SLEB, CWL) expand the range of study. Scanning speed and repetition rate enter as additional parameters and extend incident energy densities 1000 fold, and process duration 100,000 times.

By far the most widely studied application for all types of beam processing is the annealing of ion-implanted layers in semiconductors. Other applications include induced crystallization of amorphous and polycrystalline layers, pulsed diffusion of dopants directly from a surface layer, contact formation, growth and Q_{SS} reduction in oxides, surface smoothing, circuit customizing, trimming of thin films, scribing device chips, drilling and mesa formation. Recently, beam processing techniques have improved to the point that device fabrication has been attempted. To date, resistors, capacitors, diodes, bipolar transistors, MOSFETs, and solar cells have been fabricated with varying degrees of success. A representative sample of processing applications is presented in Table 1.1.

1.2 Beam-Semiconductor Interactions

Interaction of photons and electrons in solids is in itself an area of active research. However, it is appropriate that we review in general terms the important aspects of photon and electron energy deposition in semiconductors [51-53]. There are three areas of concern: energy deposition depth profile, parameters which affect this profile, and beam-induced effects.

Photons (0.1 - 5.0 eV) transfer energy to a crystalline lattice through induced vibrations of valence electrons. Reflection arises from

TABLE 1.1

EXAMPLES OF BEAM PROCESSING APPLICATIONS

APPLICATION	PROCESS USED	REMARKS	REFERENCES
-Annealing of Ion- Implantation Induced Damage/Dopant Activation			·
* Si Crystal Substrate	Ruby PL	MeV Ion-Implants EBIC Damage Invest.	1-4 5 6 7,8 8 9-11
* Si Polycrystal **Dopant B P	Dye PL Ruby PL		12 13
* GaAs Crystal Substrated **Implanted Special Te,Si,Se,Kr,Zn,l Si,Te,Se,Kr,Be	es		14-21 16-18,23
-Recrystallization of Silicon	Ruby PL ND: Yag PL Argon CWL Spire PEB SLEB	Deposited Si on Xtal Deposited Si on Xtal & Poly-xtal Subst. Deposited Si on Xtal, Lateral Epitaxy Deposited Si on Xtal Ion-Implanted Si	24 25-27 8,28-30 24 31
-Direct Doping from a Surface Layer *Si Substrates	co ₂ cwl	Photo-Induced Zone Migration	32
*GaAs Substrate	s SPIRE PEB	From AsSe Layers	33

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TABLE 1.1 (Continued)

APPLICATION	PROCESS USED	REMARKS	REFERENCES
-Contact Preparation			
*In Silicon	Ruby PL ArgonCWL	Si/CoSi ₂ /Si Contacts	34 8
*In GaAs	PEB, MSEB Nd:Yag,	Al Contacts	35
	Ruby PL	Au:Ge Contacts	36
	Argon CWL	In-Au:Ge Contacts	37
-Beam Induced Oxide Growth			
*\$1:\$10 ₂ ,\$1 ₃ N ₄	Argon CWL	O,N,C Implanted Si	38
*GaAs:Ga203	Argon CWL		39
-Oxide Charge Reduction In SiO ₂	Argon CWL		8
-Device Fabrication			
*Si Diodes			
DI DIOGES	Ruby PL	·	10
	Nd:Yag PL		40
	Argon CWL		40,41
	MSEB		10,42
	PEB		40
*Si Bipolar			
Transistors	Ruby PL	B,As,P Implanted	46
*Si MOSFETs	Nd:Yag PL	On Poly-Silicon	27
333	Argon CWL	Ion-Implanted on Xtal	47
	MSEB	11 11 11	48
*Si Solar Cells	Ruby PL	P ⁺ Ion-Implanted	49
	Ruby PL	Pulsed Diffused	50

partial reradiation by excited electrons. The remaining energy is transferred to the lattice via electron-atom collisions. For normal incidence,
power density absorbed at a depth z in a one dimensional semi-infinite
sample illuminated by a beam of intensity I is given by:

$$\phi(z) = I_{\Omega}(1-R)\alpha e^{-\alpha z} \qquad (1.1)$$

where R is the fraction of photons reflected and a the absorption coefficient. Electrons (5-50 keV), on the other hand, may interact either elastically with the atomic nuclei, or inelastically with local electrons. The elastically scattered (backscattered) electrons can reemerge from the sample with as much as 50% of the energy of the incident beam. Inelastically scattered electrons are usually modeled as losing their energy to the lattice in a continuous scattering process:

$$-dE/ds \propto (n_e/E_O) \ln(E_O/J)$$
 (1.2)

where E_O is the incident electron energy, n_e is the total density of electrons and J the ionization potential of the material. This formulation applies along the path of each beam electron. Since each electron is scattered many times, deposited energy depth profiles must account for deviation in the electron trajectory due to each collision. The results of these calculations are truncated pseudo-gaussian[52,53] distributions which are relatively independent of the beam energy when plotted as a percentage of extrapolated electron range [53]. For silicon, this range is given by:

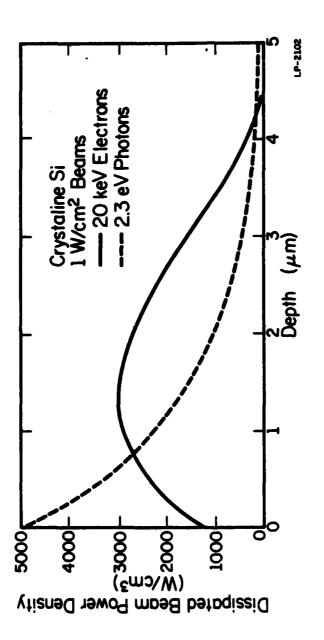
$$R_g = 4.57 E_o^{1.75}$$
 (1.3)

where E_0 is the electron energy in keV, and the R_g is given per unit density of the target material in $\mu g/cm^2$. The energy loss distributions become more skewed towards the surface of the sample as the atomic number of the target increases [52].

The probability of photon absorption is related to the density of available initial and final states of a valance electron transition. Hence, both photon absorption and reflection coefficients depend strongly upon the photon wavelength and sample temperature. In crystalline silicon, for example, α has a value of about 10^6 cm⁻¹ at wavelengths shorter than 0.4 μ m then falls rapidly to a few times 10^2 cm⁻¹ at 2 μ m, as the corresponding photon energy falls below bandgap. Most semiconductor bandgaps decrease with increases in temperature, causing the drop off in α to occur at longer λ . The degree to which a sample may have heavy disorder or ion-implantation induced damage will also increase absorption. As indicated in Eqns. 1.1 and 1.2, electron power absorption is generally only effected by material density and **mic number, with far less sensitivity to temperature. In the same way, the backscatter efficiency (η) depends primarily upon the atomic number of the target.

Figure 1.2 demonstrates the relative absorbed power density profiles in crystalline silicon for a 1 J/cm^2 flux of 2.3 eV photons and 20 keV electrons. These energies are typical of beam processing experiments. The photon profile is based upon Eqn. 1.1 with R=0.37 and $\alpha=8\times10^3$ cm⁻¹ while the electron profile uses $\eta=0.174$ and the experimentally verified energy dissipation distributions of Everhart and Hoff [53]. Although the overall depth of penetration is nearly equal, the power dissipated by electrons exceeds that of photons for most of the profile.

Under more intense laser illumination, semiconductor materials display beam-induced effects which significantly affect energy absorption [51]. Free carriers generated by the photon flux can become numerous enough to increase α by direct absorption. At higher energy densities, these



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in the electron beam case, the peak value of energy deposition occurs Theoretical energy deposition profiles for 1 W/cm² beams of 20 keV electrons and 2.3 eV photons in crystalline silicon. Notice that well within the sample. Fig. 1.2.

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carriers can produce impact ionized carriers, further increasing α . If the photons are delivered in a short pulse, electron-hole densities can become high enough to create a reflecting plasma. These hot carriers can also diffuse from the surface, significantly affecting the absorbed power profile. If heated beyond the melting point, both α and R increase, due to the metallic nature of the molten state. Since electron power absorption does not depend upon the density of electron states in the target, analogous high power effects are not significant for electron beams. Photons used in some beam processes have wavelengths equal to major fractional parts of the thickness of dielectric coatings. The result can be constructive interference and severe localized heating. Corresponding electron-dielectric effects are not possible in the scale of integrated circuit structures.

1.3 Trends in Beam Processing Technology

Semiconductor beam processing technology is still very much in a developmental state. However, enough is known about the characteristics of each technique to predict its ultimate industrial applicability. The requirements of each application will be the deciding factor.

Activation of ion-implanted dopants in single crystal semiconductors, although the most studied application, places the most severe restrictions on beam technology. Activation of the implanted species must be efficient. Residual defect concentrations must be low. Conventional sample heating either during or after beam treatment is not desirable. Although most beam processing techniques have achieved activation of dopants, a number of recent studies indicate that pulsed techniques, in which the semiconductor actually melts, produce residual defects which cannot be eliminated without post-processing furnace annealing. One might therefore imagine that

any fast melt-refreeze process would leave residual disorder at the point of furthest advance of the melt front. This seems to be borne out by recent research.

Bentini et al. [54] have demonstrated that MSEB solid phase regrowth in phosphorus implanted silicon produces better minority carrier diffusion lengths that both PEB and melt phase ruby PL processing. Anderson et al. [17] use differential resistivity techniques to demonstrate consistently larger mobility in implanted GaAs layers when CW lasers are employed. Ruby and Nd:YAG PL and the SPIRE PEB machine were compared with argon and Nd:YAG CWL. They suggest that rapid solidification may be accompanied by large concentrations of antistructural defects. They also suggest that highly non-stoichiometric regions can be created by melt phase induced arsenic evolution. Direct evaluation of defects after both melt and solid phase processing has been performed by Benton et al. [55]. DLTS studies on B^{+} and As^{+} implanted silicon show as many as 100 times (10¹¹ vs. 10^{13} cm⁻³) more residual defects in Nd:YAG PL as inCO2 CWL processed diodes. In a separate study, Benton et al. [56] use DLTS and TSCAP to identify defects in single crystal material generated directly by Nd:YAG PL induced melting. Boroffka et al. [10] have studied leakage currents in arsenic implanted silicon diodes prepared by ruby PL and scanned e-beam. They observe consistently smaller leakage by the solid phase e-beam process. Likewise, Sandow [40] reports superior I-V characteristics in arsenic implanted, argon CWL annealed diodes compared with both pulsed Nd:YAG and PEB processed devices. He suggests that the differences are due to large concentrations of residual defects remaining after the pulsed processing.

As one might expect, melt phase processing is accompanied by rapid redistribution of dopants [57,58]. This characteristic is not desirable in cases where special profiles have been established by multiple implantation, or where great control of the junction depth is necessary. This taken with the evidence about junction defects makes it unlikely that pulsed beam technology will replace standard furnace diffusion or annealing in applications where high quality or tailored profiles are required. Continuous wave lasers and multi-scanned or swept-line electron beams are the most likely candidates for this application.

In devices requiring dielectric coatings, unintentional spot heating due to laser interference effects can have a devastating effect on surface morphology [59]. These effects are not expected for electron processes. In addition, raster scanned CWL techniques have been shown to produce nonuniformities in annealing quality on the scale of the beam spot. Mizuta et al. [60] have studied As⁺ implanted CWL annealed silicon by electron beam induced current (EBIC) analysis. They observe reduced minority carrier charge collection efficiency in banded patterns parallel to the direction of travel of the beam spot. These bands are attributed to laser induced defects formed in uneven patterns beneath the implanted layer. Since spot sizes were of the order of microns, such banding can have serious effects on the characteristics of planar devices. Recently Sheng et al. [7] have extended this EBIC study to include raster scanned electron beam annealing. They demonstrate that the RSEB technique produces even less residual damage than argon CWL treatment, without the banded damage regions.

The facts outlined above seem to indicate the general suitability of electron beams for processing semiconductor material of integrated circuit complexity. When other practical considerations are taken into account, the

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SLEB technique has some merit over other electron beam systems. This method relies on a fixed line geometry beam, below which samples are translated mechanically. The requirements for scanning electronics are eliminated as are concerns for maintenance of precise focusing. On an industrial scale, wafer processing speed should be no slower than by pulsed beam processes, since mechanical translation will ultimately limit any automated beam process. Waiting time for system charging is also eliminated since the beam will run in continuous fashion.

In this work, I have explored in some detail the ability of the SLEB technique to reduce residual defects in amorphous layers and to activate ion-implanted dopants and traps. It will be demonstrated that future industrial requirements for high quality junctions are indeed met by this technique.

I do not contend that pulsed melt phase processes will be without future application. E-beam pulsed diffusion or implanted layer annealing may prove important for majority carrier devices where defects are not of concern. Since photon energy absorption can be extremely shallow, the entire area of contacts remains fertile ground for PL techniques. However, at the relative power densities and speeds at which lasers can be directed, I feel it unlikely that rastered laser techniques will ultimately be used to process devices of substantial area. Even scanned CW laser systems require as much as 10 minutes to anneal a 3 inch wafer [61]. Even longer cycle times should be expected of rastered beam systems which have significant charging times between pulses.

2. EXPERIMENTAL PROCEDURES

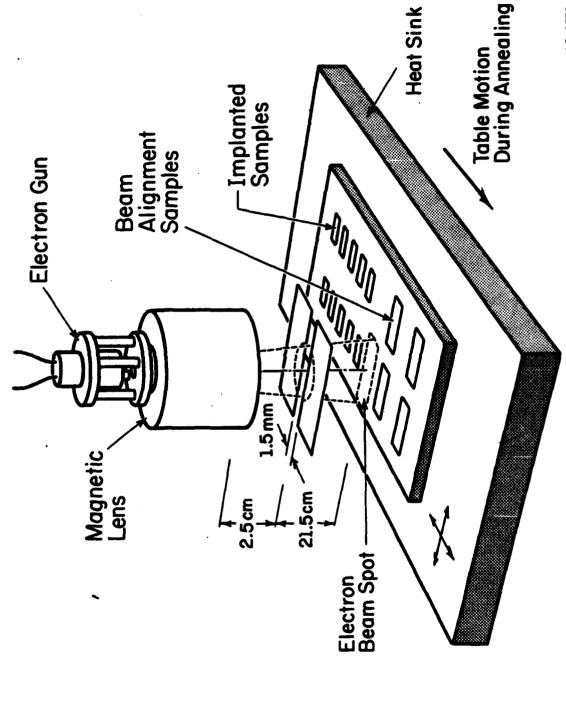
In this section, the apparatus and procedures used for annealing, implanting and characterizing semiconductor material will be discussed in detail.

2.1 Swept Line Electron Beam System

The annealing apparatus is shown schematically in Figure 2.1. The electron gun used was an Alloyed General Vacuum Model EG3-101 with modified strip filament. This gun produced a stationary, cylindrically symmetric electron beam. An electrically grounded molybdenum slit was positioned 2.5 cm below the base of the gun magnet. The beam was allowed to strike the slit in an unfocused condition. This arrangement produced a nearly rectangular electron beam spot on the grounded target plate. The shape of the beam spot could be adjusted through a combination of gun magnet setting, slit width and working distance to the target plate. Normally, a spot size of 1.0 x 1.5 cm was used.

Samples were affixed to the graphite coated molybdenum target plate with graphite adhesive suspension. This plate was attached to a 9 kg copper heat sink and placed on a motor driven X-Y translation table. Samples to be annealed under a common set of conditions were arranged in a row, with the long dimension parallel to the long dimension of the beam spot. Each row of samples was annealed in a single continuous motion of the X-Y table. The entire arrangement was enclosed in a stainless steel vacuum chamber. System pressure was reduced to 5×10^{-6} torr prior to annealing.

The electron beam was monitored by a trio of Faraday cups shown in Figure 2.2. These were arranged in a triangular array on the X-Y table. One side of this triangle was parallel to the longitudinal axis of the beam



LP-1578 Slit and target plate are at electrical ground. Alignment samples are used to center each row of experimental samples on the electron beam. (See Yu |91|.) Fig 2.1. Schematic diagram of the Swept-Line Riectron Beam Annealing apparatus (not to scale).

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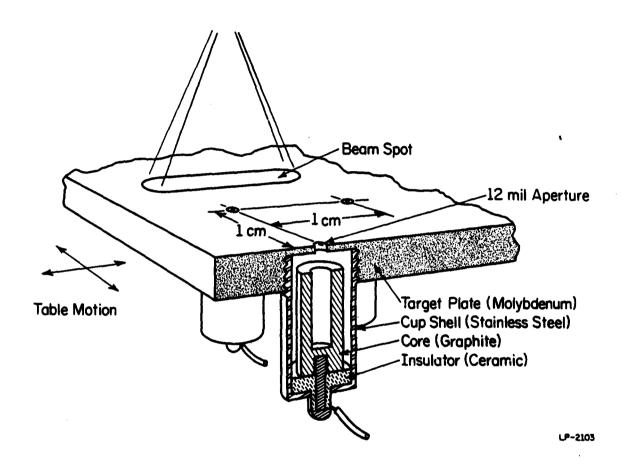


Fig. 2.2. Cut-away view of the Faraday cup beam monitor. Each cup samples a 12 mil wide line as the array is translated through the beam spot. Geometry and materials were chosen so that the cups act as near perfect electron collectors.

spot. During annealing, the array was translated through the beam spot. Collected cup currents were monitored continuously with a Keithley Model 410CR electrometer and strip chart recorder. These records were used to obtain beam energy density profiles and table translation speed.

Each cup was designed to capture nearly all incident electrons [62]. Secondary and backscattered electrons generated within the cups could have have introduced considerable measurement error. The secondary electrons, normally defined as those with energy less than 50 eV, [52,63] were easily captured by a small attractive potential applied to the cup cores. The backscattered electrons, however, could have possessed a significant fraction of the incident beam energy [64]. With rough coated graphite for core material, backscattered electron yield was reduced to less than 8% of the incident flux [52]. The re-entrant geometry of the cores ensured capture of most of those actually generated. I estimate no more than 2% of the incident electrons escaped capture.

2.2 Ion Implantation

All implantation was performed on the CSL Accelerators Inc. model 300-MP, shown schematically in Figure 2.3. $^{28}\text{Si}^+$ and $^{11}\text{B}^{19}\text{F}^+$ ions were generated by cold cathode discharge from SiF_4 and BF_3 gas sources respectively. Previous studies have shown that the Si beam created with this source will contain less than 10% residual N_2^+ [65]. This species cannot be removed by mass analysis. A considerably larger percentage of N_2^+ could be expected if the hot cathode and SiH_4 gas source were used. $^{9}\text{Be}^+$ ions were also generated with the cold cathode, their source being a solid Be canal insert which is continuously sputtered by BF_3 gas discharge. $^{14}\text{N}^+$ ions for GaAsP implantation were generated by hot cathode discharge of N_2 gas.

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Schematic diagram of the Accelerators Inc. MP-300 ion-implantation system. (After Rosa | 122 |.) Fig 2.3.

All samples were mounted 7° off beam normal to reduce channeling effects during implantation. GaAsP samples were mounted in the target chamber with conductive paint. Silicon samples were mounted by direct pressure contacts to avoid contamination associated with the adhesive. Si samples amorphized by self-implantation were mounted on a liquid nitrogen cooled finger. The front surface temperature of these samples was monitored with a thermocouple probe.

Perfluorinated polyether diffusion pump fluid was used in the target chamber during all implantations. This fluid was found to reduce surface carbon contamination of implanted material [65]. This was particularly important for low temperature implantation, in which residual gases condense on the cold sample.

2.3 Methods of Characterization

2.3.1 SEM channeling pattern analysis

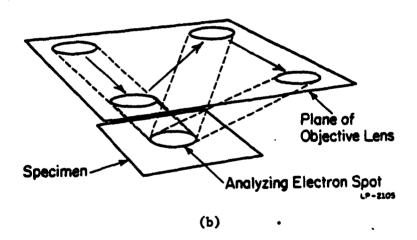
Determination of lattice orientation and qualitative evaluation of crystal perfection were made with scanning electron channeling pattern analysis. A JOEL JSM-35C scanning electron microscope was used. This system was equipped with Selective Area Channeling Pattern (SACP) electronics. Electrons normally used for imaging were analyzed for Bragg backscattering. The resulting patterns represented crystal characteristics only for the area analyzed by the electron spot. Since this spot could be as small as $10~\mu m$ diameter, tiny crystallites and disordered regions could be detected.

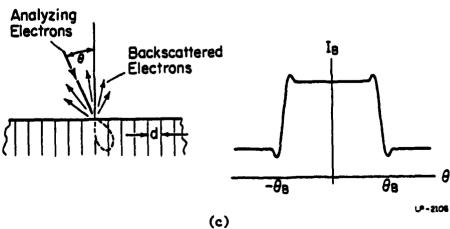
When operated in the SACP mode, the microscope's electron beam is altered to produce a highly parallel beam [66] (See Figure 2.4a). The beam is rocked and swept about a fixed point as shown in Figure 2.4b. If the specimen is crystalline, the condition for Bragg backscatter will be satisfied

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Fig 2.4. (a) Schematic diagram of the JEOL JSM 35C SEM beam optics with channeling pattern electronics activated. Field limiting aperture and lower deflection coils are added. (b) The resulting beam rocking is shown here highly exaggerated. (c) Variation in the first Bloch wave backscattered electron current. A large change in this current occurs when the Bragg condition is met.







at certain points in each scan described by:

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2d
$$\sin \theta_b = n \lambda_e$$
 $n = 1, 2, 3, ...$ (2.1)

Here, d is the crystal plane spacing, $\lambda_{\bf e}$ is the electron wavelength and $\theta_{\bf b}$ is the Bragg angle (see Figure 2.4c). The resulting variation in backscattered electron signal is displayed in conventional video fashion.

The crystallographic orientation of each sample area can be determined from its characteristic channeling pattern [67]. Also, the spacings of lattice planes may be determined from the width of the interference pattern lines as given by:

$$d = c\lambda_{\rho}/D \tag{2.2}$$

where D is the SACP line width and c is a constant for fixed SACP mode magnification and electron energy [66].

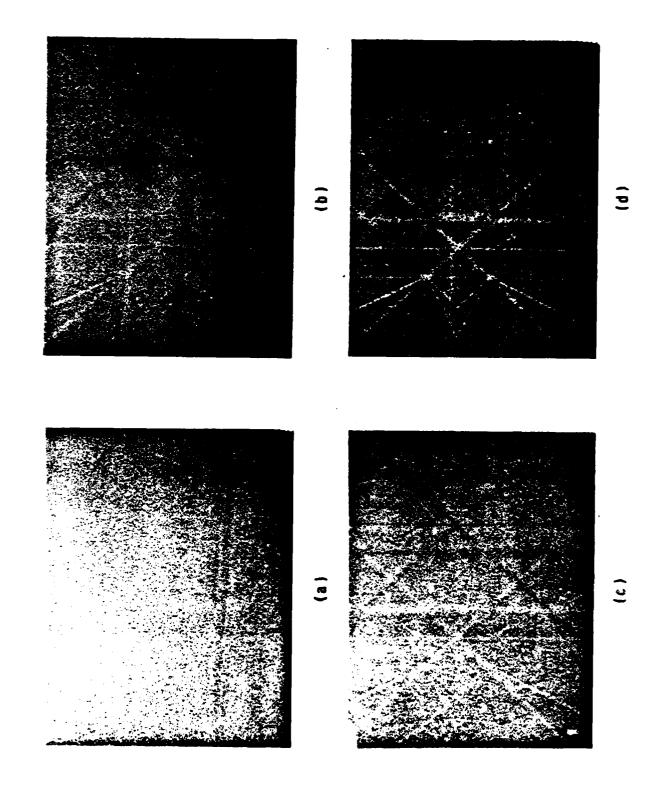
One would expect the quality of a SACP to indicate the degree of a sample's crystal perfection. This is clearly shown in Figure 2.5, which is a succession of SACPs recorded at different points across an amorphous-crystal interface created by partial annealing. As the analyzing spot is moved across the interface (Figure 2.5a to 2.5d), the channeling pattern lines related to the low order crystal planes become visible. In the figure, these are the lines which appear most nearly vertical. Finer detail appears as the beam moves onto undamaged material. The compositional sensing mode of the SEM is used here, which tends to wash out the horizontal interference lines.

It has been shown that an amorphous film as thin as 200 Å, covering an otherwise crystalline sample, will introduce sufficient interference to wash out a SCAP [67]. Physical surface defects such as scratches, stress

Fig. 2.5. Selective Area Channeling Patterns recorded at four points across an amorphous-crystalline interface in silicon. The amorphous material shows no channeling (a). Lower order lattice lines (those most nearly vertical and horizontal appear first (b and c). Finally in crystalline material (d), fine line structure becomes clear.

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marks or etch pits also degrade SACP quality. Thus, transient annealed material must have both good crystal order and good surface morphology to produce highly detailed channeling patterns.

2.3.2 Deep level transient spectroscopy

2.3.2.1 Overview and apparatus description

Deep Level Transient Spectroscopy (DLTS) was used in this work to detect and analyze semiconductor defects. The theoretical basis for DLTS has been well established: [68,69] however, I will briefly review the relevant fundamental concepts. Basically, DLTS operates through analysis of transient capacitance decay of a reverse biased diode. An example for majority carrier traps in the depletion layer of a p - n diode is illustrated in Figure 2.6. The device under test is held at a quiescent reverse bias. The traps are initially free of electrons. A short bias reducing pulse is applied which compresses the depletion region, allowing the traps to fill. Immediately after the pulse ends, the junction capacitance falls below its quiescent value C, by an amount ΔC due to the compensating charge of the filled traps. Electrons are then thermally emitted from the traps, and the capacitance returns to its quiescent value. The characteristic time of the capacitance decay depends primarily upon the ratio of the trap activation energy and device temperature. By measuring this decay time as a function of temperature, the energy level of the defect may be inferred. The magnitude of the capacitance change ΔC is a measure of the concentration of defects. By adjusting the magnitude of the bias reducing pulse, one may determine the distribution of a particular defect. The trap capture cross section can be obtained from a measurement of ΔC with varying bias reducing pulse width. If the bias reducing pulse magnitude is increased so as to cause actual

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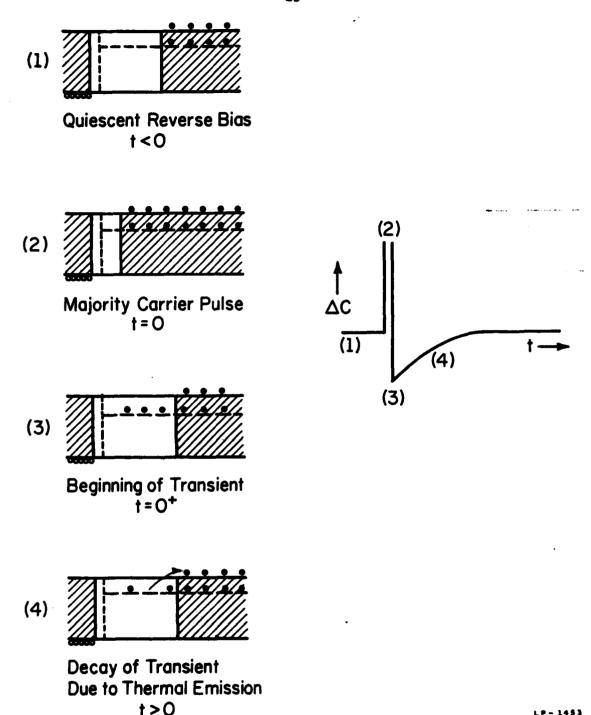


Fig. 2.6. Capacitance transient due to a majority carrier trap in a p'-n diode. Inserts labeled 1-4 schematically show the junction depletion layer (shaded region) and charge state of the defect as the transient occurs. (After Lang | 68|)

injection, DLTS will detect minority carrier traps in the same way. The sign of ΔC determines whether majority or minority carrier traps are being analyzed. It can be seen that DLTS is a powerful technique for the detection and analysis of semiconductor defects.

The DLTS system used in this work was developed by D. S. Day et al. [70] and is shown schematically in Figure 2.7. This system employs a unique two-arm bridge circuit. Each arm contains a diode of similar C-V and I-V characteristic. These are mounted on a common TO-18 header and held within a variable temperature dewar. This arrangement keeps differences in device temperature to a minimum. The bridge is driven by a 20 MHz modulating signal. The device labeled "Test Diode" is driven exactly 180° out of phase with the "Dummy Diode". Shifts in the characteristics of the test device tend to be cancelled by the dummy device, and the entire bridge remains in balance during temperature scanning. Note that the DC quiescent bias is applied to both devices, while only the test device receives the bias reducing pulse. Isolation from this transient pulse is provided by two attenuators, a power splitter, a phase shifter and bandpass filter. We may therefore assume that only the test device produces a Δ C signal.

The bridge signal is demodulated at the HP mixer, amplified and finally detected at the lock-in amplifier. A special gate circuit eliminates the large capacitance overshoot present during the bias reducing pulse. This prevents amplifier overload and keeps system response time limited to less than 1 μ sec. The magnitude of ΔC is displayed on the X-Y recorder as a function of device temperature. A Booton 76-3A standard capacitor is used in place of the diodes to align the bridge to the capacitive mode and to provide calibration.

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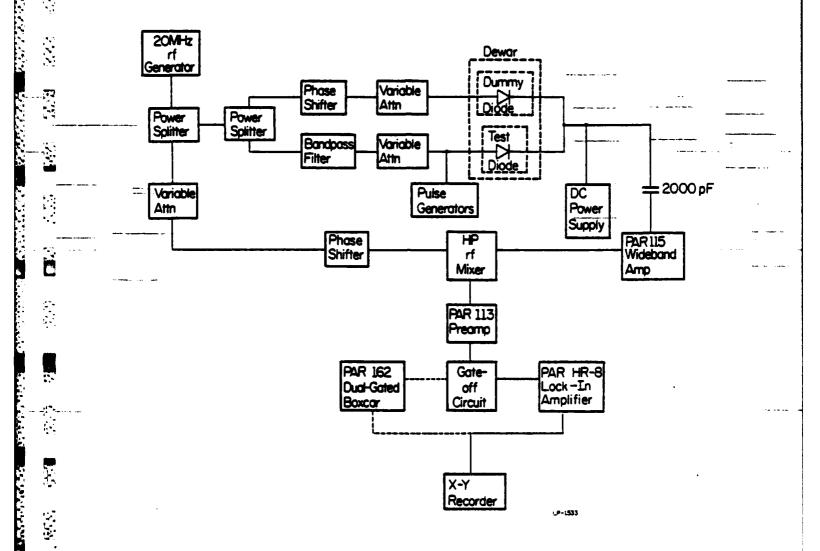


Fig. 2.7. Block diagram of the two-diode DLTS System. (After Day | 70|)

2.3.2.2 DLTS data analysis

In this work, only the energy level of the traps and their concentration profiles were studied in detail. The manner in which this information was obtained from DLTS data is summarized in this section and in Appendix A.

From the principle of detailed balance and carrier statistics, the emission rate of carriers from a trap (e), can be expressed in terms of its capture cross section (σ), the trap degeneracy factor (g), the rms thermal velocity of the captured carrier ($\langle v \rangle$), the appropriate effective density of states (N) and the depth of the trap in the bandgap (ΔE)[69]. For the case of electron traps (and adding appropriate subscripts);

$$e_n = \frac{\sigma_n < v_n > N_c}{g} \quad \exp \left(-\Delta E/k_B T\right) \tag{2.3}$$

If one assumes no temperature dependence of the capture cross section, (valid for certain types of traps) and using:

$$N_c = 2M_c \left(\frac{2\pi m^* k_B^T}{2}\right)^{3/2}$$
 (2.4a) $\langle v_n \rangle = \left(\frac{3k_B^T}{m_c^*}\right)^{1/2}$ (2.4b)

we may write:

$$\frac{1}{\tau_n} = e_n \propto T^2 \cdot \exp(-\Delta E/k_B T)$$
 (2.5)

where τ_n is the time constant corresponding to this emission rate. Finally,

$$T^2 \tau_n \propto \exp\left(\frac{\Delta E}{k_R T}\right)$$
 (2.6)

Thus a plot of $\ln(T^2\tau_n)$ vs 1/T will yield a line whose slope is proportional through known constants to ΔE . τ_n is determined by the fundamental frequency

set on the lock-in amplifier. T is the temperature at which a trap produces the largest ΔC signal. Each trap can be analyzed at several different frequencies, and least squares fit to these data can then be made to improve accuracy [71].

The actual magnitude of the capacitance transients ΔC must be calculated from the output of the lock-in amplifier. This output is the time average of the product of the input signal and the lock-in's square wave weighting function. Both the shape of the input waveform and its phase with respect to the weighting function will affect the value of ΔC detected. In this work we follow the analysis of Day [71,72]. The input waveform is assumed to be a train of simple exponentially decaying spikes. The weighting function is adjusted to be in phase with the leading edge of the bias reducing pulse (bias-pulse phase reference method). Under this condition, mathematical analysis of the detection process yields the expression:

$$\Delta C = 0.560 \times S_L \times S_B \times V_L$$
 (2.7)

where ΔC is the transient capacitance in pF, S_L is the lock-in sensitivity in volts, S_B is the calibration factor in pF/V and V_L is the lock-in output in volts.

From these values of ΔC , one may construct a profile of defect density. If one considers the example of a p⁺-n diode, Lang has determined [73]

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$$\delta\left(\frac{\Delta C}{C}\right) = \left(\frac{\epsilon}{qW^2N^+}\right) - \frac{N_T(x_c)}{N^+(x_c)} \delta V_c \qquad (2.8)$$

where C and W correspond to the diode capacitance and depletion width while quiescent reverse bias V is applied. δ $(\frac{\Delta C}{C})$ is the change in the $\frac{\Delta C}{C}$ ratio between two successive measurements, with bias reducing pulse V and

 V_c + δV_c . N^+ is the fixed charge concentration (due to ionized donors in our example) at the n edge of the depletion layer. $N_T(x_c)$ and $N^+(x_c)$ are respectively the densities of traps and of fixed charge at the location (x_c) of the depletion layer edge during the bias reducing pulse $(v_c + \delta V_c)$. A trap profile may be constructed via a series of measurements of ΔC while varying V_c , with fixed V. To be valid, $\Delta C << C$ and traps must occur only on the n-side of the junction. It must also be assumed that the acceptor and donor concentrations change in the same ratio on both sides of the metal-lurgical junction. This assumption is valid for linearly graded and step junctions.

The fixed charge profiles were produced via point-by-point capacitance voltage measurements. A Hewlett Packard 6114A precision power supply provided bias to a Booton 72B capacitance meter for these measurements. A sufficiently small interval in voltage was placed between measurements to estimate $\mathrm{dC/}_{\mathrm{dV}}$. The magnitude of fixed charge concentration was determined via the expression:

$$N(x) = \frac{C(y)^3}{\epsilon q A^2 (-dC(V)/dV)}$$
 (2.9)

The depth x was determined by numerical integration of the fixed charge concentration profile and knowledge of the device geometry (See Appendix A, Section A.2, lines 19800-21800).

Trap profile analysis, including determination of the fixed charge profile, was accomplished by computer. The FORTRAN program TRAPSI was developed specifically for Schottky barrier diodes on n-type silicon. This code is described in detail in the appendix.

2.3.3 Differential resistivity and Hall effect measurements

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Profiles of electrically active implanted dopants were established by differential resistivity and Hall effect measurements made in conjunction with chemical layer stripping. The apparatus was developed by McLevige et al. [74], and is shown schematically in Figure 2.8. This double AC Hall system possessed high sensitivity, good noise rejection and inherent averaging of misalignment and thermoelectric effects. During Hall measurements, the samples were placed in an AC electromagnet which was driven at one fourth the basic system frequency (f_1) of 1 kHz. Via a mixer and filter, a f_1 - f_2 signal was generated which formed the lock-in reference signal for the Hall voltage. f_1 was used as the lock-in reference for resistivity measurements.

Samples were prepared by the technique described by Tsai [65]. The carrier type of the substrate was choosen so that a p-n junction was formed after implantation and annealing. First a 120 mil square van der Pauw mesa pattern was photolithographically defined and plasma etched. Gold contacts were then evaporated and later sintered at 300°C in flowing dry H₂. Samples showing good junction characteristics were selected so that only the implanted layer contributed to the measurement. After each measurement, a thin layer of the sample was removed by chemical etching. A series of wax defined mesas were formed on each sample during thinning. The heights of these mesas were later measured by Detak mechanical stylus to establish the depth scale. The thinning and measurement process was continued until the samples became too resistive to measure.

The sheet resistivity (ρs), and sheet Hall coefficient (R_s), are calculated from [75]:

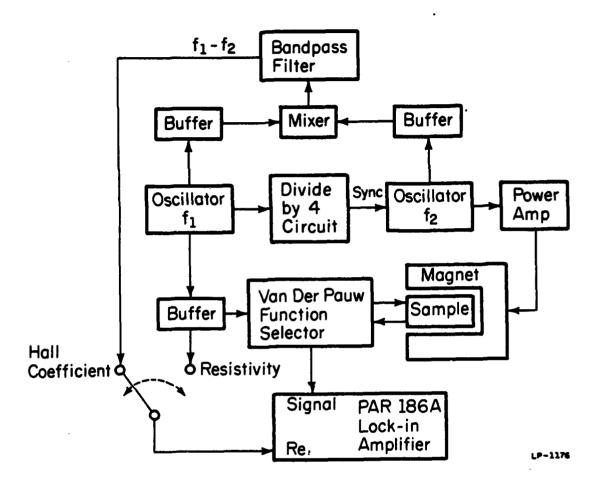


Fig 2.8. Block diagram of the double AC Hall apparatus. (After McLevige et al. |74|)

$$\rho_{s} = \left(\frac{\pi}{\ln 2}\right) \cdot \frac{V_{ABCD} + V_{BCDA}}{2I} \cdot f\left(\frac{V_{ABCD}}{V_{BCDA}}\right)$$
 (2.9)

$$R_{s} = \frac{\sqrt{2} \Delta V_{BDAC}(rms)}{B(rms) I(rms)}$$
 (2.10)

Here the designation V_{ABCD} corresponds to the voltage between contacts A and B with current I passing between contacts C and D, and similarly for V_{BCDA} . $^{\Delta}$ V_{BDAC} is the change in Hall voltage induced by placing the sample into the magnetic field of strength B. The correction factor f ($\frac{V_{ABCD}}{V_{BCAD}}$) has been tabulated by van der Pauw [75].

The average mobility and carrier concentration of a particular layer j of thickness d_i are given by: |76|

$$\gamma \mu_{j} = \mu_{H_{j}} = \frac{R_{s_{j}}}{\rho s_{j}} + \frac{R_{s_{j-1}}}{\rho s_{j-1}} - \frac{R_{s_{j-1}} - R_{s_{j}}}{\rho s_{j-1} - \rho s_{j}}$$
(2.11)

and

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$$n_{j} = \frac{\frac{1}{\rho_{s_{j}}} - \frac{1}{\rho_{s_{j-1}}}}{ed_{j}\mu_{i}}$$
 (2.12)

The designation j-l refers to the preceeding layer. γ is the ratio of Hall (μ_{H_j}) and conductivity mobility (μ_j) . Its value was taken to be 0.73, which is appropriate for the highly doped p-type silicon layers studied here [77].

3. SLEE ANNEALING OF Si -IMPLANTED AMORPHOUS SILICON

This chapter presents a comparative study of amorphous ion-implanted silicon recrystallized by swept-line electron beam and conventional furnace annealing. Solid phase recrystallization of amorphous silicon has been studied previously using furnace techniques |65,78,79|. Dopants implanted in high doses can be efficiently activated with accompanying recrystallization at relatively low temperatures (approximately 550°C). As demonstrated by Tsai et al. |80|, however, electrical profiles of these dopants can include an electrically in active tail due to heavy residual implantation damage. (See section 4.1) This layer is located between the bulk material not damaged by the original implantation and material which regrows completely during annealing. In a p-n junction, this damage coincides with the depletion region, and will adversely affect leakage currents and minority carrier lifetimes.

Tsai et al |81 have also shown that the location of the residual damage can be pushed well beyond the p-n junction by amorphizing the sample (eg., by Si⁺ ion implantation) to a depth beyond the implanted dopant profile. Samples prepared in this manner have completely active dopant profiles. In fact, fluorine migration to defects |81| has shown that the unannealed damage is moved to the tail of the deep amorphizing implantation.

The presence of this damage was further confirmed through a preliminary study using silicon solar cells. This work was undertaken in cooperation with Dr. J. Eguren of the Instituto De Energia Solar, Madrid, Spain. A set of n⁺pp⁺ back surface field cells was fabricated with and without the use of amorphizing self-implantation. Here the low-hi (pp⁺) region is meant to reduce the back surface recombination velocity. The Ė

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front surface n⁺ layers were formed by conventional furnace diffusion.

Some of the samples then underwent multiple low temperature Si implantation to produce a continuous amorphous back surface layer. A single room temperature gallium implant was then made in all the samples to form the back surface p⁺ layer. The energy of this implantation was sufficiently low that all gallium atoms remained well within the amorphous layer. After furnace annealing, the solar cells were characterized under Air Mass 1 illumination.

Representative results are shown in Table 3.1. These data show consistently better performance in cells which were not pre-amorphized. Samples 1.2-1.4 show generally smaller open circuit voltage (V_{oc}) and short circuit currents ($I_{f,b}$) when compared with sample 1.1. Implantation and annealing conditions were such that one would expect a completely active gallium layer in the pre-amorphized cells and only partial activation of gallium in the unamorphized cells. This alone would lead one to expect just the opposite of the observed difference in performance. The result can be explained in terms of reduced cell base lifetime, due to the self-implantation induced damage. The study described below will characterize this damage in some detail.

DLTS is used here to directly evaluate residual crystal damage. The experiment is simplified through the use of Schottky barrier diodes fabricated on recrystallized self-implanted material. Ambiguities of p-n junction dopant-defect complexes are thus eliminated. Since Schottky diodes can be prepared without disturbing the bulk crystal, a direct comparison of SLEB and furnace recrystallized material can be made.

TABLE 3.1

AMI RESPONSE DATA

Ga +- IMPLANTED S1 SOLAR CELLS

0027202

Sample	Pre-	Dose (cm ⁻²)	Annealing Temp/Time	T (mk)	(ae) f	(mA)	q (90)
	2	3.75x10	600 C/30 min	31.7	549	4.9	495
1.2	Yes	1.56x10 ¹⁴	550°C/30 min	34.2	459	3.5	352
1.3	Yes	3.75×10 ¹⁴	550°C/30 min	27.1	400	3.1	330
_	Yes	3.75×10^{14}	550°C/30 min	26.2	391	2.8	340

Comparative response data for Ga-implanted Si solar cells prepared with and without amorphizing Si -implantation of the back surface. The designations b and f refer to measurements made with back and front surfaces illuminated. Note the generally smaller values of I and $^{
m V}_{
m OC}$ observed in the predamaged cells, especially during back surface illumination.

3.1 Experimental Procedure

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Devices used in this study were fabricated from $0.24~\Omega$ -cm (4 x $10^{16}~cm^{-3}$), phosphorus doped Czochralski grown bulk silicon. This level of dopant was chosen to provide the best compromise between Debye length limits on profile resolution and the requirement for full depletion of the regrown amorphous layer during measurement [83]. As in the solar cell experiments described above, the samples received four cold (\lesssim -100°C) amorphizing implants with Si⁺ ions of energies 32, 91, 158 and 255 keV. These energies and the corresponding doses were chosen to give the best fit to an ideal 0.5 μ m deep, flat implanted profile of 1 x $10^{20}~Si^+/cm^3$. Etching experiments [81] determined the depth of the amorphous layer to be 4550 $\frac{N}{r}$ 125 $\frac{N}{r}$.

Samples were then recrystallized either by the SLEB process or by conventional furnace annealing. The electron beam annealing process was described in section 2.1. An electron energy of 20 keV and table translation speed of 0.32 cm/sec were used in this work. A second set of samples was thermally annealed in a quartz-lined furnace tube under a forming gas ambient. Unimplanted material was heat treated simultaneously to detect defects which might be introduced during furnace annealing and unrelated to the implantation.

After annealing, the front surfaces of the samples were anodically oxidized [65] to remove a 200 Å layer of Si, exposing clean surfaces for Schottky barrier formation. Al Schottky barriers and Au-Sb ohmic back-side contacts were formed by vacuum evaporation through shadow masks. Individual devices were cut, mounted on headers, and thermocompression lead bonded. Sample heating did not exceed 300°C for 10 minutes during this processing.

Defect energy levels and profiles, as well as profiles of fixed charge were measured and calculated by the methods described in section 2.3.2 and the appendix. With the exceptions noted below, measured values of $\Delta C/C$ were between 10^{-2} and 10^{-5} , satisfying the restriction that $\Delta C/C <<1$ [68,69]. 3.2 Results and Discussion

DLTS spectra are presented in Figure 3.1 as a function of 30-minute isochronal furnace annealing. The DLTS signal is plotted logarithmically, with majority carrier signal increasing along the vertical scale. The peak trap signal decays as the regrowth temperature is increased, as expected. In each case, the spectra are dominated by two defect signals. The lower temperature signal (corresponding to $E_{\rm c} - 0.22$ eV) appears in all three cases and becomes dominant as annealing temperature is increased. The higher temperature trap signal changes from $E_{\rm c} - 0.50$ eV to $E_{\rm c} - 0.35$ eV to $E_{\rm c} - 0.42$ eV as the annealing temperature is increased. Defects with activation energies within ± 0.02 eV of these four trap signals have been observed in implanted [84], irradiated [85,86], or laser damaged silicon [87]. Defect spectra for control Schottky barriers fabricated on unimplanted but simultaneously annealed Si show no detectable defect signal.

at three peak beam power densities. There is a marked reduction in the peak trap signal from lowest to highest power density. The dominant signal peak of the well-annealed SLEB case (38 W/cm²) is about a factor of four smaller than the smallest peak in the 800°C case of Figure 3.1. The designation "x2" refers to a sample which was annealed by two passes of the beam. Notice that the double annealed sample at intermediate power density (27.5 W/cm²) shows the largest over-all defect signal spectra. The thermal

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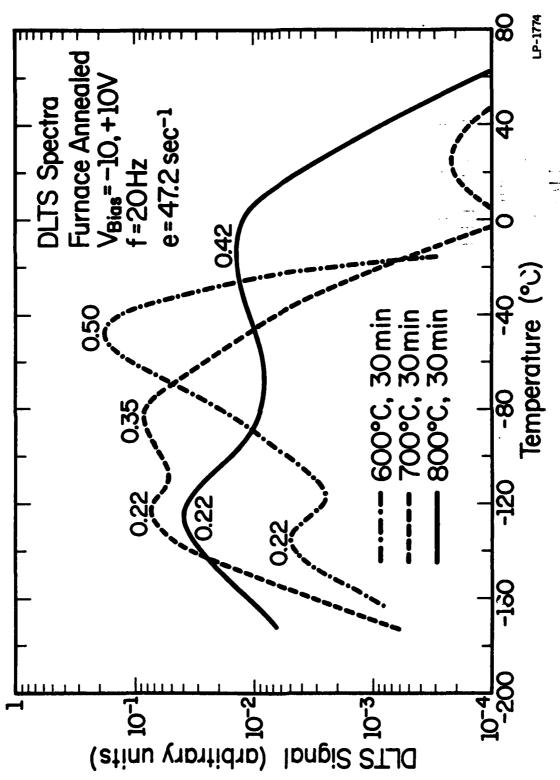
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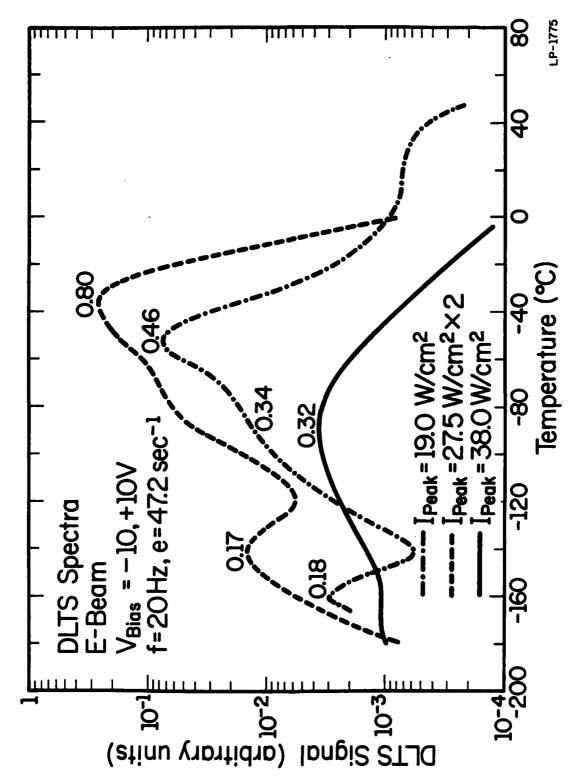
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Majority DLIS spectra for Schottky barriers fabricated on furnace annealed silicon. carrier signal is plotted on the logarithmic vertical scale. (See Soda 31). F18. 3.1.



DLTS spectra for samples annealed by SLEB for three power densities. The vertical scale has units identical to figure 3.1. (See Soda |31|.) Fig 3.2.

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activation energies observed in the SLEB case, with the exception of E_c - 0.34 eV, do not correspond to those observed in the furnace case. Activation energies within \pm 0.02 eV of the observed levels E_c - 0.17 eV, 0.18 eV, 0.34 eV, and 0.46 eV, have been previously observed in implanted [84], irradiated [85,86], or laser damaged [87] silicon. The level E_c - 0.80 eV has not been reported previously.

Profiles of fixed charge and defect concentration for the furnace annealed devices are presented in Figures 3.3 and 3.4. In each case, the profiles are dominated by a layer of defects and fixed charge near the original amorphous-crystalline interface (marked by the arrow). The magnitude of these effects decays with increased annealing temperature. Also observed is a relatively small concentration of defects in the near surface regions. This is accompanied by a tendency for fixed charge concentrations to return to values corresponding to the original bulk dopant concentration $(4 \times 10^{16} \text{ cm}^{-3})$.

In the 700°C and 800°C cases, the defect profiles reach a maximum at 0.42 to 0.45 µm respectively, corresponding to the measured thickness of the original amorphous layer. This observation verifies the location of damage reported by Tsai et al. [81,82] from their Hall profiling and fluorine decoration studies. Previous studies in irradiated material also indicate that the near surface recrystallized regions tend to have fewer defects [88], as observed here.

The fixed charge profiles presented here must include the contributions of both ionized donors and defects [83]. In regions where the defect concentrations become comparable to the fixed charge profiles, one cannot strictly interpret the latter as a donor profile. Rather, the fixed charge profile represents N_d+nN_T , where n and its sign depend upon the charge state

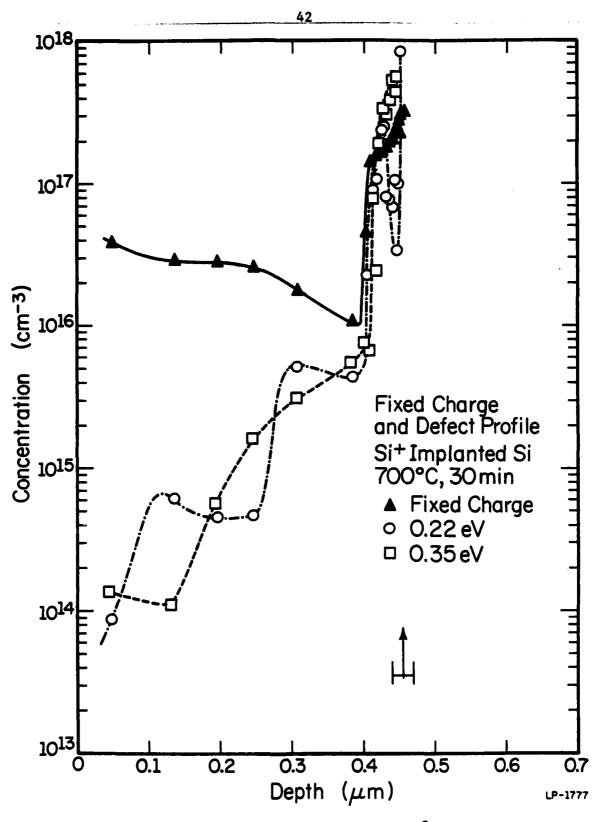


Fig. 3.3. Fixed charge and defect profiles for 700°C furnace processed silicon. The arrow indicates the location of the original amorphous-crystalline transition region. (After Soda | 31|.)

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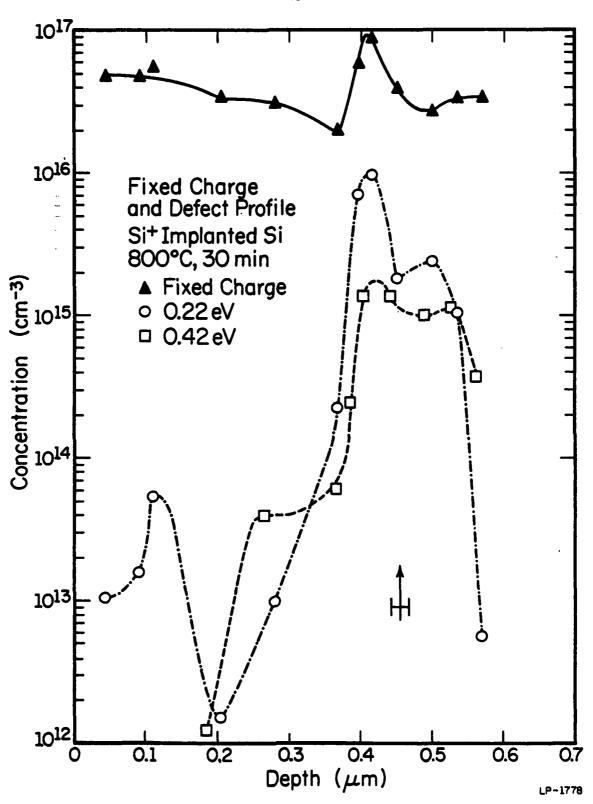


Fig. 3.4. Fixed charge and defect profiles for 800°C furnace annealed material. Note the change in vertical scale from Fig. 3.3. (See Soda |31|.)

of the defect. This is important in the 700°C case near the peak damage region. In the 800°C case, however, ionized donor charge predominates and we see definate donor redistribution, particularly in the neighborhood of the original amorphous-crystalline interface. The donor redistribution effect can be understood in terms of a dissociative diffusion process of the type proposed by Baruch [89]. Motion of dopants is explained by a pair of competitive processes in which a defect will first liberate a donor atom from its lattice site, then cause the donor to move by attraction to another defect site. The donor atom undergoes a net motion in the direction opposite the motion of defects. These processes are used to explain bulk dopant redistribution and peaking in proton irradiated silicon [89]. The shapes of the donor profiles in the near-surface region suggest dopant motion toward the interface region.

It is likely that the solid phase regrowth process itself is involved in the redistribution of both defects and donor atoms, especially in the 600°C case (not shown). A reasonable extrapolation of previously determined solid-phase epitaxial regrowth rates [78] indicate that nearly 25% of the total annealing time was required to recrystallize the amorphous layer in this case. The advancing crystal front seems to push defects ahead of it, accelerating the motion of dopant atoms and leaving a bulge in the defect profiles near 0.23 µm. Regrowth times are estimated to be factors of 14 and 370 times faster respectively for the 700° and 800° anneals shown here. No bulge in the defect profile is observed in the regrown regions of Figures 3.3 and 3.4, indicating that either the crystal front has moved too rapidly to push the defects, or they have annealed extensively after regrowth is complete.

Defect and fixed charge profiles for swept-line beam annealed material are shown in Figures 3.5 and 3.6. In both cases, the residual defect concentrations are small enough that one may interpret the fixed charge profiles as due entirely to ionized donors. After a single sweep by a 19 W/cm² electron beam, the sample exhibits a series of broad, relatively flat defect profiles (not shown). Surface channeling pattern analysis shows that annealing in this case is insufficient to completely regrow the amorphous layer.

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Recent studies of nitrogen implanted GaAs $_{1-x}P_x$ |91| have suggested that multiple scanning with SLEB can improve crystal quality without defect migration. This possibility was explored in the 27.5 W/cm 2 sample (Figure 3.5), which was double annealed. In this case, severe dopant redistribution occurs. Electron microscope channeling analysis shows complete recrystallization was not achieved. Since the 0.80 eV defect Δ C/C signal is so large (\approx 0.1), its profile is doubtful. Some surface dopant out-diffusion is observed. A large misalignment of the defect and donor peaks with the amorphous-crystal interface is observed, probably due to a near surface donor depleted region which cannot be analyzed by C(V) measurements. We believe the depth scale is affected, and that the peaking of defects and charge in Figure 3.5 actually occurs at the original interface (marked by the arrow).

The threshold for complete crystal growth is crossed in the 38 W/cm^2 case (Figure 3.6). SEM analysis shows perfect near surface crystal order. Both dopant redistribution and out-diffusion effects are minimized. The profile of the single defect observed in this case (E_c - 0.32 eV) occurs

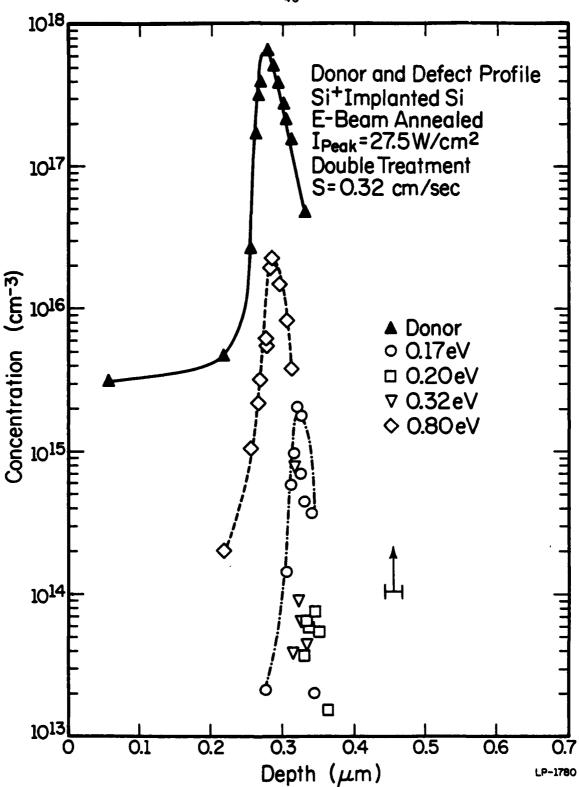


Fig. 3.5. Donor and defect profiles for SLEB annealed silicon processed with two passes of a 27.5 W/cm beam. (After Soda |31|.)

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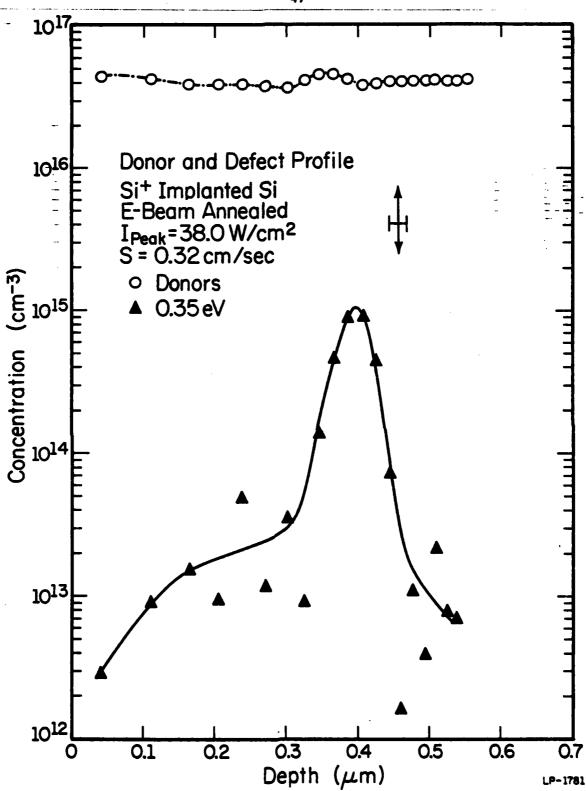


Fig. 3.6. Donor and defect profiles for 38 W/cm² SLEB annealed silicon. Note the change in vertical scale from fig. 3.5. (See Soda |31|.)

at about the depth of the original amorphous-crystalline transition. Peak defect concentrations are a factor of ten smaller than in the 800°C furnace annealed case, while near surface defect densities are a factor of five to ten smaller.

Other studies of recrystallization of amorphous Si by pulsed E-beam processes [92] explain the regrowth strictly in terms of beam induced heating. In this work, total annealing times on the order of two seconds were used. These are considerably longer than either pulsed [92] or raster scanned [93] E-beam processes. Therefore, the annealing conditions are somewhat more similar to those observed to cause MeV electron or keV proton irradiation induced defect annealing. In these studies, TEM techniques [94,95] and IR absorption [96] are used to observe both crystal regrowth and accelerated defect annealing.

Geranismenko [97] has suggested that point defects generated by higher energy electrons can be responsible for decay of relatively stable defect formations, such as those observed in this work. These defects are thought to compensate or induce migration of the defects responsible for the original amorphous state. He also suggests that the electron induced ionization may change the charge state of the defects, increasing their mobility.

It would seem that generation of point defects by electrons of only 20 keV is a minor effect. The lower limit for electron induced atomic displacements is 145-200 keV [98,99]. However, Hinkley [100] has invoked a two-step energy transfer process to explain subthreshold defect generation in silicon. In this process, incident low energy electrons excite valence electrons, producing plasmons. These plasmons transfer their energy to the

lattice, eventually causing atomic displacements. The plasmon process also explains an experimentally observed [100] reduction in this threshold with increasing sample temperature. Since the SLEB produces sample heating, the plasmon process may contribute to the observed reduction in residual defects, such as observed in Figure 3.6.

Some support for this theory comes from comparison of peak trap concentrations of the beam annealed samples. If a strictly thermal regrowth and annealing process were responsible, one would observe a steady overall reduction in the trap concentration as beam power is increased. Double annealing should accelerate this trend. In fact, the largest peak trap concentrations and significant donor redistribution are observed in the 27.5 W/cm² double sweep case, which was certainly warmer during the second beam sweep. In this case, plasmon induced defects could explain the accelerated donor migration. No major donor redistribution effects are observed in samples treated with a single sweep.

3.3 Conclusions

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The data show that relatively deeply amorphized Si layers can be recrystallized by swept-line electron beam processing. DLTS analysis shows that SLEB can reduce residual defect densities to levels well below that achievable by conventional furnace annealing. This is particularly true in the transition region between bulk and recrystallized material, where residual damage is resistant to high temperature annealing. It is significant that SLEB recrystallization can be effective without the use of additional furnace treatment. SLEB processes can also reduce bulk dopant redistribution effects which occur during furnace regrowth. These results do not represent the

best quality recrystallized material achievable, but they do demonstrate that SLEB processing can be a viable and effective alternative to rastered spot or pulsed area annealing techniques.

4. SLEB ANNEALING OF BF TIMPLANTED SILICON

This chapter extends the study of SLEB recrystallized amorphous silicon to include BF₂⁺ implanted Si, in which the amorphization is created by the fluorine and acceptor doping is provided by the boron. Hall and Secondary Ion Mass Spectroscopy (SIMS) profiling reveal high electrical activation efficiency and only modest spatial redistribution. Unlike furnace annealed material, active boron is observed in the as-implanted amorphous-crystalline transition region. This can be important to the production of high quality implanted p-n junctions. Distribution effects of implanted fluorine are also explored, and these migration effects suggest that SLEB annealing does not produce crystal damage beyond the original implanted profile.

4.1 Experimental Procedure

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The samples used in this study were Czochralski grown, phosphorus doped, 0.24 Ω -cm, <100> silicon. Implantation of BF $_2^+$ ions was performed at 150 keV to a fluence of 1 x 10 15 cm $^{-2}$ at room temperature. These conditions have been found sufficient to create an amorphous layer \sim 1325 $^{\circ}$ thick [80]. Beam annealing was accomplished as described in section 2.1. Samples of dimensions 1 x 1.3 cm were attached to the sample stage and translated at 0.32 cm/sec during annealing. An electron energy of 20 keV was used in this study.

After annealing, gold contacts were applied and a van der Pauw geometry mesa was defined by photolithographic techniques and plasma etching. Each slice accommodated either six or eight Hall patterns. Heat cycling after SLEB annealing did not exceed 300°C for 15 sec. Electrical carrier profiling was accomplished by double AC Hall measurements in conjunction with

chemical layer stripping, as described in section 2.3.3. Etch depths were measured at various points in the profile by using a Sloan Dektak mechanical stylus.

Samples used in electrical profiling measurements are subsequently used in SIMS profiling, to facilitate comparisons between atomic and electrically active profiles. Gold contacts were removed exposing processed implanted silicon which was uneffected by the electrical characterization. A maximum of 65 mils separated the regions which were electrically and chemically profiled. Secondary ion mass spectrometry was then performed using the Cameca AMS 3F ion microprobe. 0^+_2 ions of 14.5 keV were employed for sputtering. Mass 11, 19, 28, and 31 signals were monitored during each profile by peak switching techniques. Concentration scales were established through reference to an unannealed standard. A Tencor mechanical stylus was used to measure crater depths and thus establish the depth scale.

4.2 Results

SLEB annealing was performed at power densities of between 19 and 64 W/cm². SEM channeling pattern analysis indicated that all samples annealed in this range attained high quality near surface crystal order. Those annealed at the lowest power density, however, were too resistive to be Hall profiled. The net active carrier profiles for the three electron beam power density conditions are shown in Figure 4.1. The designation "X3" means that the sample was passed below a beam of the indicated power density three times. A ninety second interval was allowed between successive sweeps under the beam. We observe a general increase in the peak active boron concentration as the annealing power density increases from 30 to 64 w/cm². The 64 w/cm² profile compares favorably with the as-implanted SIMS atomic

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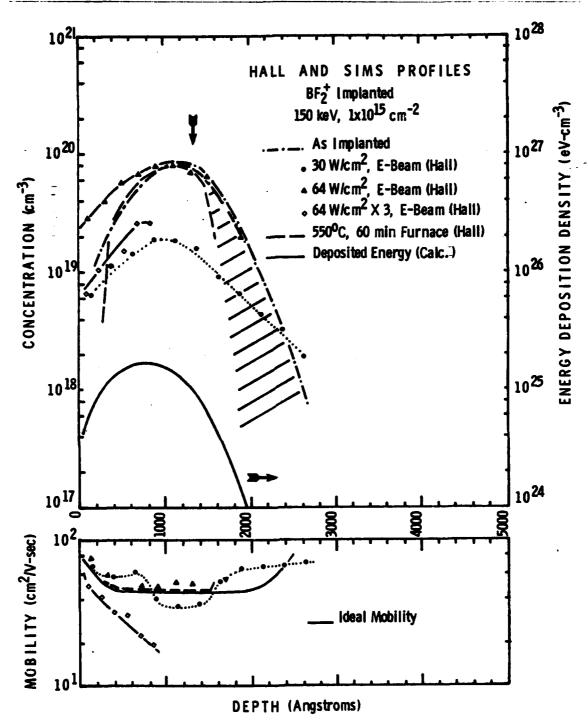
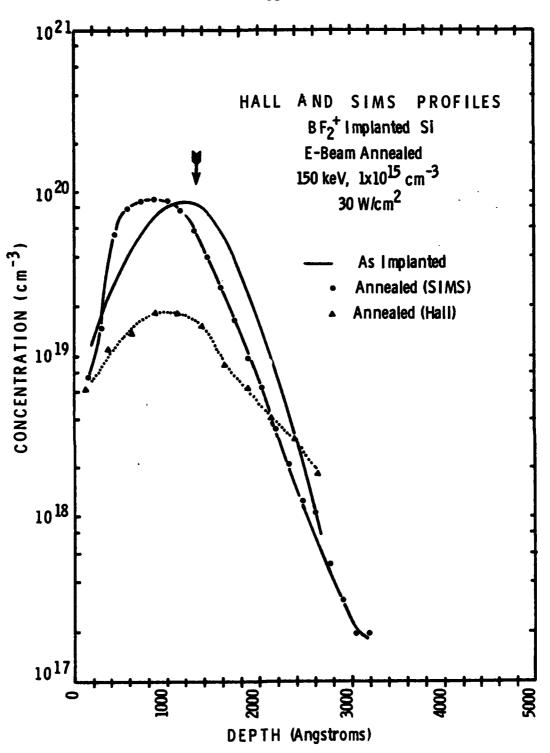


Fig 4.1. Net acceptor concentration and conductivity mobility profiles for BF₂ implanted silicon annealed at three SLEB power densities. Shown for comparison are the as-implanted atomic boron and corresponding "ideal" mobility profile. The furnace annealed profiles are due to Tsai et al. |80|. The calculated energy deposition density due to the implantation is also shown (right hand scale). The arrow marks the as-implanted amorphous-crystalline interface (see text).

boron profile except at depths less than 600 Å, where the electrical profile is larger by a factor of 2-3. After a triple sweep at 64 W/cm², the profile decays and becomes unmeasurable beyond 825 Å. Also shown are conductivity mobilities calculated assuming $\mu_{\rm c}=0.73~\mu_{\rm H}$. The solid curve corresponds to mobilities achieved in bulk material at the concentration of the as implanted atomic profile [77, 101,102]. Only the triple sweep profile deviates significantly from this bulk mobility profile.

Figure 4.1 includes an electrical profile measured by Tsai et al. [80,81] in low temperature furnace annealed material, otherwise prepared under identical conditions. In the region beyond about 1400 Å, they observe an inactive tail (shaded region). This tail was found to correspond to the region which was heavily damaged, but not driven amorphous by the implantation. The original amorphous-crystalline boundary is marked by an arrow in Figures 4.1-4.5. In the SLEB annealed sample, relatively high levels of activation are measured out to 1900 Å, well into the inactive tail observed previously. In the 30 W/cm² sample, we find boron activation out to 2600 Å, nearly twice as deep as observed in 550° C furnace annealed material.

The actual distribution of boron is revealed in Figures 4.2-4.4. Here the electrical data of Figures 4.1 are compared with the as-implanted and beam annealed atomic profiles as measured by SIMS. The 30 W/cm^2 annealed material shows a very definite skewing while the electrical profile indicates poor activation efficiency. Activation becomes nearly complete in the 64 W/cm^2 case (Figure 4.3), where the SIMS and electrical data come into good agreement. The discrepancy between electrical and atomic profiles at depths shallower than 1100 $\text{\^{A}}$ is within combined measurement errors. Note that this atomic boron profile is skewed away from the as-implanted profile much less



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Fig. 4.2. As-implanted and annealed SIMS profiles for material processed at 30 W/cm². The net acceptor profile is included for comparison. Note the poor activation efficiency and shift in the SIMS profile towards the peak of damage.

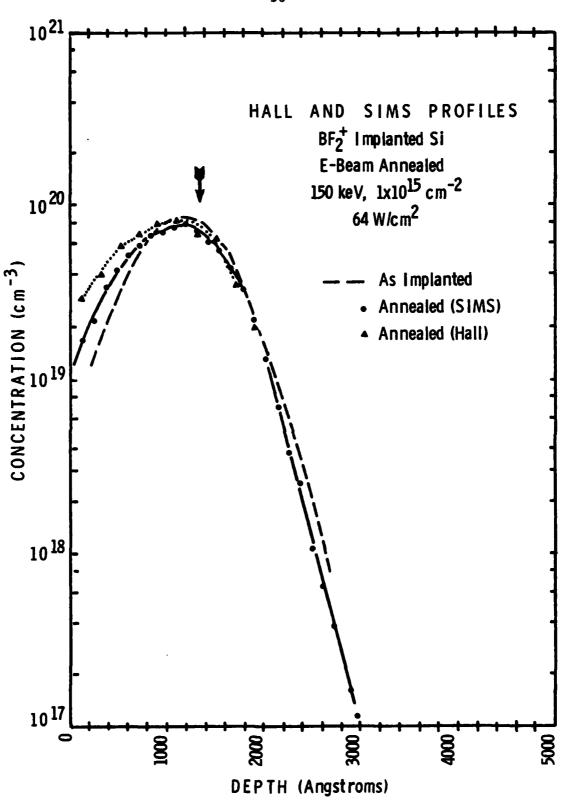


Fig. 4.3. SIMS and electrical profiles as in figure 4.2, but for material processes at 64 W/cm. Activation of boron is nearly complete with only minimal redistribution.

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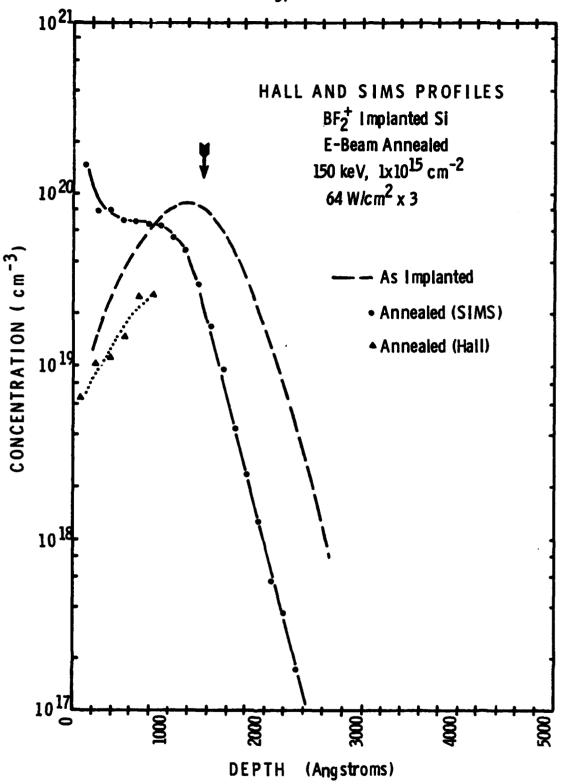


Fig. 4.4. SIMS and electrical profiles as in figure 4.2, but for triple pass, 64 W/cm beam annealed material. Migration becomes significant. Near-surface activation efficiency is poor.

than is the corresponding profile in the 30 W/cm^2 case. Also note that the atomic boron concentration at depths less than 400 Å actually exceeds the 30 W/cm^2 profile by factors of as much as 2. A much more pronounced surface accumulation effect occurs in the triple sweep case (Figure 4.4). This accumulation is accompanied by a large shift in the tail of the distribution toward the sample surface.

Similar SIMS profiles of implanted fluorine are presented in Figure 4.5. The beam annealed fluorine curves possess the general shapes of the corresponding boron SIMS profiles, with one rather striking exception. The 64 W/cm² profile shows an abrupt spike of fluorine, peaking at about 1300 Å. Also shown is a fluorine profile measured by Tsai et al. [82] in material which was identically implanted but furnace annealed at 900°C for 30 minutes. This furnace annealed sample has a fluorine profile with two peaks, centered about the peak of the 64 W/cm² E-beam annealed profile.

4.3 Discussion

boron in the original amorphous-crystalline transition region is perhaps the most significant. This can be understood in terms of the study of celf-implanted amorphous silicon discussed in chapter 3. The data show that under proper conditions the defect concentration in the transition region can be reduced to levels below that achievable even by high temperature furnace processes. This explains the ability of the SLEB process to activate boron in this damaged region, as demonstrated in the 30 and 64 W/cm² cases. Recall from chapter 3 that annealing conditions producing reduced residual damage also produced minimal redistribution of dopant atoms. This accounts for the reduced skewing effects observed in Figure 4.3 as compared with

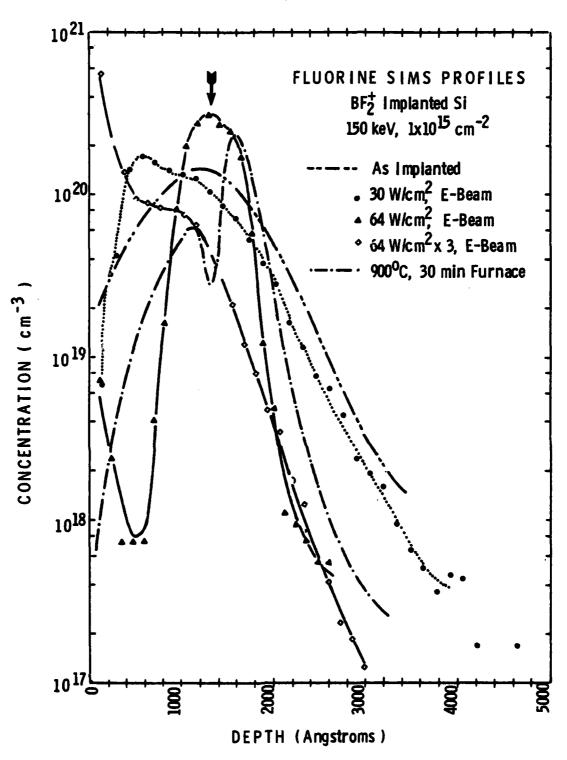


Fig. 4.5. Fluorine atomic profiles for as-implanted and SLEB annealed material. The 900°C, 30 min furnace annealed profile of Tsai et al. |82| is included for comparison. Note the large accumulation of fluorine at the original amorphous-crystalline transition region in the 64 W/cm² case.

Figure 4.2. In the latter case, defects have remained more numerous, resulting in the depressed electrical activity and poor mobility observed in the region 600-1600 $^{\circ}$ A. At even lower power density (19 W/cm²), defects are so numerous that no activity can be detected at all.

In the 30 W/cm² case of Figures 4.1 and 4.2, it appears that the boron activation efficiency increases significantly in the region beyond 2200 $^{\circ}$ A. This occurs despite depressed boron activity in the regrown region shallower than 1600 $^{\circ}$ A. This effect can be explained by considering the energy deposition density profile of the implantation [65,102]. (Also shown in Figure 4.1.) At a depth of 2000 $^{\circ}$ A, the deposited energy has fallen by a factor of 10 from its value at the amorphous-crystalline interface. One should therefore expect a precipitous drop in the pre-annealing defect density in this region. The increased boron electrical activity is thus at least partially due to a local increase in the pre-annealing crystal quality.

energy profile (and therefore the peak of the as-implanted damage profile) is shallower than the peak of the as-implanted atomic boron profile.

(800 Å vs 1390 Å). It was shown in chapter 3 that in both furnace and SLEB annealed silicon, dopant atoms tend to migrate to areas of high defect density. All of the SLEB annealed profiles show a shift toward the peak of the calculated damage profile, the most prounounced effect occuring in the 30 W/cm² SIMS profile of figure 4.2. This is expected, since the most residual damage should occur in a sample annealed at lower beam power density. An analogous shift in the furnace annealed profile of Tsai et al.[80,81] is present in figure 4.1. In this case, however, dopant migration is also influenced by the motion of the amorphous-crystalline interface and by residual damage in the original interface region.

The study of self-implanted silicon (chapter 3) shows that large concentrations of defects and heavy migration of bulk dopant atoms into the as-implanted interface region occur in multi-sweep SLEB annealed material. This effect explains the triple sweep profile (figure 4.4). Heavy residual damage results in depressed values of mobility and the large near surface atomic boron concentration, due to migration of boron to this damage. Migrating bulk phosphorus atoms can compensate implanted boron atoms, depressing the active profile.

Verification of phosphorus migration by SIMS is difficult because of a large background mass 31 signal due to SiH. The lower limit of SIMS phosphorus detection is estimated to be 3×10^{20} cm⁻³. Therefore, effects of phosphorus redistribution during annealing may be studied indirectly. For example, we note that the annealed SIMS boron profile of figure 4.4 falls with increasing depth, while the electrical profile climbs. This alone would imply a general decrease in defect density, which should be associated with an increase in mobility. We observe, for example, that the 30 W/cm² mobility proflie improves between 100 and 600 Å, and beyond 1600 X (figure 4.]), where the electrical and SIMS profiles are in better agreement. In contrast, the triple sweep mobility profile (figure 4.1) falls continuously. If a significant quantity of electrically active donors were present within the measured profile, compensation of the boron acceptors would occur, along with a decrease in mobility, as observed here. The fact that this effect occurs in the triple sweep case is consistent with the observation in chapter 3 that donor migration is most severe in multisweep annealed material.

Fluorine redistribution effects in furnace annealed BF implanted silicon have been explained in terms of recrystallization-induced migration,

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gettering by radiation damage, and thermal outdiffusion.[82] recrystallization times are short in beam annealing processes, one would expect only the latter two factors to be significant in this study. Motion of the amorphous-crystalline interface influenced the damage and dopant profiles of only the lowest temperature furnace annealed sample (section 3.2). The shifting of the 30 W/cm^2 fluorine profile (figure 4.5) can be explained in terms of gettering at the same residual implantation-induced damage we believe responsible for the corresponding boron redistribution. At 64 W/cm², the lack of fluorine at depths shallower than 1100 A seems to indicate that much of this implantation-induced damage has been annealed away. The more stable damage at the as-implanted amorphous-crystalline interface dominates the fluorine migration in this case. There is excellent agreement between the location of the SIMS fluorine peak of this work and that of the as-implanted interface measured by Tsai et al.[80-82] (depth 1325 \Hat{A}). These authors previously accounted for the two peak nature of the furnace annealed fluorine profile by the motion of the interface region during recrystallization. As mentioned above, we do not observe such dual peak phenomena in E-beam annealed material. Tsai et al.[65] have also demonstrated that fluorine gettering effects are strongest on the bulk side of the as-implanted interface. The slight skewing of the 64 W/cm2 profile coincides with their observation.

In the multi-sweep case, the same damage-aided diffusion effect responsible for the large surface boron concentrations appears to produce the observed fluorine distribution. Although fluorine outdiffusion appears likely, the present studies do not demonstrate this conclusively. The

flattening of the multi-sweep curve between 500 and 1000 Å tends to indicate that some residual as-implanted interface damage may still be affecting the final fluorine distribution.

Finally, it should be noted that the tails of the fluorine profiles move progressively closer to the surface with increasing E-beam treatment. Furnace annealing studies[81] have shown that radiation damage will effectively getter fluorine, even if it is as much as 3000 Å deeper than the peak of the as-implanted fluorine profile. Therefore, it is unlikely that any significant regions of damage exist deeper than the peak of the as-implanted fluorine profile to the limit of the deepest SIMS analysis (7000 Å). We contend, therefore, that even triple sweep SLEB does not produce bulk damage beyond the as-implanted profile.

4.4 Conclusions

At the lowest power levels studied have, electron beam heating is sufficient only to grossly reorder the lattice. At higher annealing power, the defect density is reduced sufficiently to produce partial electrical activation. The residual damage from the implantation strongly influences the final atomic distributions. Under more intense beam conditions, this residual implantation damage is more completely annealed and diffusion effects become less influential. The more annealing-resistant damage at the original amorphous-crystalline transition region strongly getters implanted fluorine. Finally, under miltiple sweep annealing conditions, the beam induces large defect concentrations in the region shallower than the peak of the implanted profile. Damage aided diffusion processes skew the profiles toward the surface. The possibility of some bulk dopant involvement and of actual outdiffusion exists, but cannot be confirmed through this study.

The data are consistent with recrystallization and dopant activation in amorphous, BF_2^+ implanted silicon by swept line electron beam annealing. Under proper conditions, acceptor profiles with good electrical activity and mobility are observed, and redistribution effects are minimized by the use of SLEB annealing. This study also demonstrates that SLEB processing can produce electrical activity in the amorphous-crystalline transition region, which has not been achieved by low temperature furnace processes. The influence of residual radiation damage on the redistribution of the implanted species is consistent with that observed in furnace annealed material. Our results show that SLEB annealing does not produce bulk lattice damage out to 5000 $^{\circ}_{\rm A}$ beyond the peak of the as-implanted profile.

5. SLEB ANNEALING OF GaAs_{1-x}P_x

In this chapter the investigation of SLEB annealing is extended to include the $GaAs_{1-x}^P$ system. This technique can effectively activate implanted dopants and the nitrogen isoelectronic trap with minimal redistribution of impurities or implantation related damage. In the first half of the chapter, annealing effectiveness will be explored with photoluminescence techniques. The second half will be devoted to characterization of $GaAs_{1-x}^P$ p-n junctions.

5.1 Study of SLEB Annealed GaAs Px: N by Photoluminescence

SLEB annealing effectiveness was studied initially by photoluminescence techniques. This effort was pursued in cooperation with Dr. T. Yu.[91] The relative ease of evaluation allowed a large range of annealing parameters to be explored. The relative strength of band-edge and nitrogen trap related emissions were used as a measure of annealing effectiveness. Stripping techniques were used to evaluate migration of nitrogen and implantation related damage.

5.1 Experimental procedures

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VPE layers of (100) orientation, grown on n^+ GaAs (for x=0.4,0.5) or n^+ GaP (for x=0.65) substrates. Epitaxial layer thicknesses of approximately 120 μ m included a 20-50 μ m graded composition region. The surface of the x=0.4 and 0.5 material was chemically etched to a depth of 3 μ m to ensure uniform crystal composition. The 20 μ m just below the surface of the GaAs_{0.35}P_{0.65} layers were doped with nitrogen during growth. This

doped layer was etched away on samples to be used in N-implantation studies.

The photoluminescence emission from all of the etched surfaces was measured prior to implantation for reference.

Nitrogen ($^{14}N^+$) implantations were performed at room temperature at 200 keV as described in section 2.2. Ion doses were chosen to produce peak concentrations of 10^{17} - 10^{20} cm⁻³, as determined by LSS calculations.[104] Prior to electron beam annealing, 1000 Å of $5i0_2$ was deposited on the implanted surface by the oxidation of silane. Depositions were typically performed at 450°C for 6 min.

Electron beam annealing was performed as described in section 2.1. In this study, the beam energy was maintained at 20 keV, and the table translation speed at 0.25 cm/sec. Actual on-sample beam power densities were not measured. Rather, total electron current leaving the $gun(I_b)$ was used as a relative measure of beam strength.

Conventional furnace annealing was performed on similar samples for comparison. SiO₂ films of thickness 1500 Å were deposited on both sides of these samples to prevent decomposition during high-temperature processing. Annealing was performed in flowing high-purity argon in a silica-lined furnace. Each anneal required 30 minutes at selected temperatures from 600° to 1000° C. These procedures for furnace annealing of N-implanted GaAs_{1-v}P_v have been discussed in detail previously.[105-110]

Prior to photoluminescence measurements, the protective oxides were removed with 30% HF. Samples were then mounted in a Janis "Super Varitemp" gas exchange liquid-helium cryostat and held at 5 K. The photoexcitation was provided by the 4880 Å line of a Coherent Radiation 52-G Ar ion laser. An average incident power density of 10³ W/cm² was used.

The front surface luminescence signal was focused onto the slit of a 1/2-m Spex 1302 double grating monochromator, and was detected by an RCA C31034 (extended S-20 response) photomulitplier using lock-in amplifier techniques. The emission spectra are uncorrected for system response.

Successive layer removal required for the profiling study was accomplished by chemical etching with a solution of 5 $\rm H_2SO_4$: 1 $\rm H_2O_2$: 1 $\rm H_2O$. The etching time was controlled to remove layers ~ 600 Å thick. Actual thicknesses removed were determined by Dektak mechanical stylus measurements of selective etched steps.

5.1.2 Results and discussion

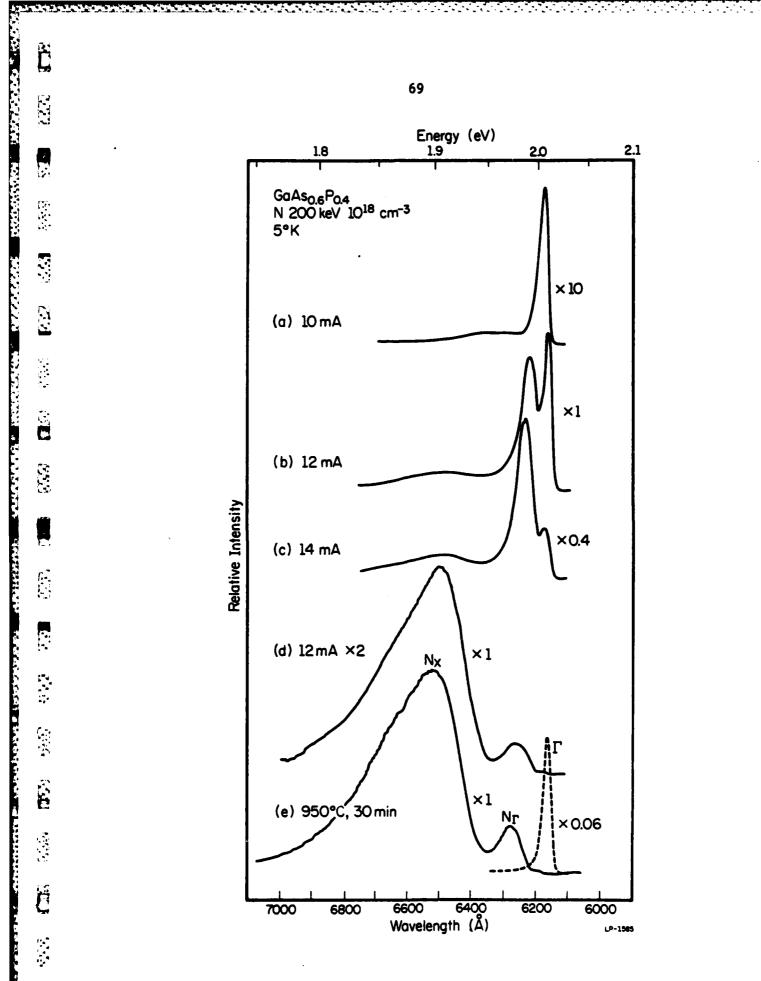
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5.1.2.1 Direct gap composition, x=0.40

Photoluminescence spectra for $10^{18} {\rm cm}^{-3}$ nitrogen implanted samples as a function of annealing electron beam current (I_b) are shown in figure 5.1. We observe as much as a 30 Å variation of the near band-edge emission across any given sample owing to slight variations in alloy composition. This accounts for the small peak misalignments observed in spectral data. Shallow donor band-edge emission Γ (λ = 6160 Å) becomes significant after annealing with $I_h=10\,$ ma (curve a). As the annealing current is increased, strong nitrogen activation is indicated by an increase in $N_{\Gamma}(\lambda=6250 \text{ Å})$ [105,106] and $N_{\chi}(\lambda=6500 \text{ Å})$ [105-108] emission. At I_{b} =15 mA, we observe localized surface melting and a reduction of emission from these melted areas. We observe, however, that significant increases in N, emission are possible with two sweeps of the beam with $I_b=12$ mA. N_x emission becomes dominant (curve d) and total integrated emission becomes comparable to that of the best furnace annealed samples (curve e). Annealing characteristics of samples with peak nitrogen concentrations of 1019 and 10²⁰ cm⁻³ are similar.

Fig 5.1. Photoluminescence spectra of GaAs_{0.6}P_{0.4} nitrogen implanted to a peak concentration of 10 cm and swept-line electron beam annealed at the indicated total beam current (I_b). Emission from unimplanted nitrogen free material is shown for comparison (dashed line). (After Yu |91|.)



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For peak nitrogen concentrations of 10^{17} cm, the maximum emission is observed after a single annealing pass at $I_b=12$ mA. The N-induced emission intensity increases slightly with increasing I_b or multiple sweeping, while the total integrated intensity remains the same. This suggests that much of the lattice disorder introduced by implantation has been removed at $I_b=12$ mA, but that larger I_b is necessary for efficient nitrogen activation.

The data for total integrated emission intensity versus furnace annealing temperature agree generally with those observed by Anderson et al. [109,110] The integrated intensities from samples electron beam annealed under optimum conditions ($I_b=12$ mA, two passes) are comparable or superior to furnace annealed samples at their individual optimum conditions. This is true for all peak concentrations of implanted nitrogen. A high degree of nitrogen substitution is evident in the case of 10^{19} cm, $^{-3}$ for which total integrated emission exceeds that of unimplanted direct-gap materials.

5.1.2.2 Indirect gap composition, x=0.50

The annealing characteristics of indirect-gap $GaAs_{0.5}^{P}_{0.5}^{O}$ are very similar to those obtained for direct gap x=0.40 material. A weak D_{0}^{X} (λ =5970 Å, exiton bound to neutral donor) emission appears after annealing with I_{b} =10 mA. As the annealing current is increased, the N_{x} emission (λ =6350 Å) strengthens until it saturates after a double anneal at I_{b} =12 mA (curve d). Integrated intensity obtained under this annealing condition is comparable to that obtained from optimum furnace annealing (950°C, 30 min). This trend holds for all nitrogen concentrations studied here.

The spectral shapes observed are essentially the same as furnace annealed samples for all nitrogen concentrations studied.

5.1.2.3 Indirect gap composition, x=0.65

Similar annealing studies were performed on $GaAs_{0.35}^{P}_{0.65}$ samples. D_{0}^{X} emission (λ =5810 Å) and N_{x} emission (λ =6010 Å) become strong under the same annealing conditions as observed in x=0.4 and 0.5 material. Again we find optimum E-beam annealing to produce N_{x} emission intensity comparable to optimum furnace annealed samples. We also find the peak intensity of 10^{19} cm⁻³ implanted material to exceed that obtained from similar material doped with nitrogen during growth. This demonstrates the effectiveness of the electron beam process in nitrogen activation and damage annealing.

5.1.2.4 Optical depth Profiling

Depth profiling studies[91] were performed on x=0.4 and 0.5 material with peak nitrogen concentrations of 10¹⁸ cm.³ The x=0.65 material was not studied because of its unsatisfactory etching characteristics. Figure 5.2 shows total integrated emission intensity for both annealed and unannealed profiles with x=0.4. Annealing conditions were chosen to produce maximum integrated emission. Variation in intensity was found not to exceed 20% across any etched region.

The unannealed x=0.4 material produces no detectable emission until the first 20 µm have been removed. Band-edge Γ emission is observed to increase until 0.58 µm, where the intensity recovers to the level of the unimplanted material. The damage profile for this implantation is predicted by Brice[103] to have an asymmetrical shape peaking at 2600 Å. The damage remaining at 0.58 µm should be only 9% of the peak damage. Our measurements show that the damage profile before annealing is no deeper than predicted. For annealed samples, the total photoluminescence emis-

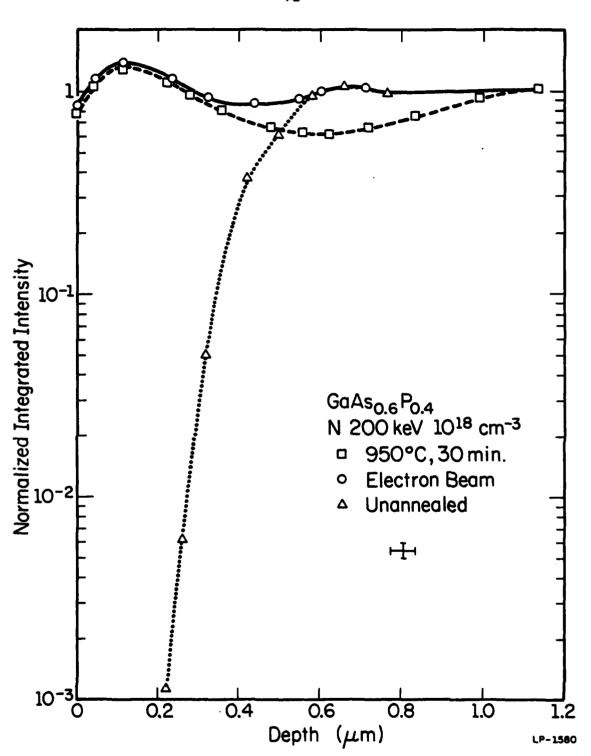


Fig 5.2. Depth dependence of the total photoluminescence intensity (5°K) of GaAs 6 Po.4 nitrogen implanted to 10°cm peak concentration. Dashed curve corresponds to furnace annealed material (950°C, 30 min), and solid line to SLEB annealed material (I = 12 mA, double pass). Data are normalized to unimplanted, unannealed nitrogen-free material. (After Yu | 91|.)

sion intensity in the first 0.2 µm is found to be comparable with that of the unimplanted materials, owing to the high concentration of active nitrogen in this region. Beyond this point emission decreases, with recovery to the level of unimplanted material occuring at 0.6 and 1.2 µm, respectively, for the electron beam and furnace annealed samples. The same general trend is found in x=0.5 material. These dips are due to a combination of reduced nitrogen concentration and residual implantation-induced damage. The unannealed sample shows no significant emission degradation at depths of 0.6 to 1.2 µm. The degradation of the furnace annealed samples in this same region may therefore be attributed to diffusion of defects. The short duration of the electron beam anneal prevents significant damage diffusion, as demonstrated by the more rapid recovery of emission with depth into the sample.

In addition to providing information about defect distributions, these optical profiling measurements can be used to study the effects of annealing on the implanted nitrogen profile.[109] The photoluminescence intensities obtained after successive etch steps depend upon the overlap of the optically generated excess carrier distribution and the nitrogen profile. The active impurity profiles may be deduced approximately if the excess carrier profile is known. Here we use the expression of $\delta p(x)$ due to Williams and Chapman.[111] For x=0.4 material we take $\alpha(\lambda=4880\ \text{Å})=4.2\times10^4\ \text{cm}^{-1}$ for 5^0K . For x=0.5, we take $\alpha(4880\ \text{Å})$ to be 3.3 x $10^4\ \text{cm}^{-1}$ at this same temperature.[91] The diffusion lengths are expected to be very short compared to the absorption lengths due to rapid irapping at the

N center and the effects of lattice damage. We use a radiative lifetime for the N-trap to be about 100 ns[112], a surface recombination velocity of 5 x 10^5 cm-s⁻¹, and a diffusion length of \sim 0.2 μ m.

The measured N_x emission profiles for x=0.4 and 0.5 material are shown in figures 5.3 and 5.4 respectively. Also shown are the theoretical N_x emission profiles based on the overlap of the estimated excess carrier distribution and a simple Gaussian as-implanted nitrogen distribution (R_p =3700 Å, ΔR_p =1150 Å) predicted by LSS theory. This computed profile has a peak at ~ 1200 Å for both x=0.4 and 0.5 compositions. There is good agreement between the theoretical active nitrogen profile and the electron beam annealed profile. The N_x emission in both x=0.4 and 0.5 E-beam annealed material ceases abruptly after removal of the implanted layer. This is consistent with the minimal diffusion expected in solid phase transient annealing which has been demonstrated in chapters 3 and 4.

Although active nitrogen profiles for the furnace annealed samples reach a peak at the same depth as the E-beam annealed samples, they display detectable N_x emission to depths of 0.8 and 1.2 μ m respectively, for x=0.4 and 0.5 material. For x=0.4 material, 0.8 μ m actually represents the point where we are no longer able to discern N_x emission above the donor-acceptor pair and N_r emission. Since we observe N_r emission to a depth of 1.2 μ m in the x=0.4 case, it is likely that nitrogen has diffused as deeply as in the x=0.5 composition material. Since pair emission is negligible in the case of indirect material and there is no N_r inter-

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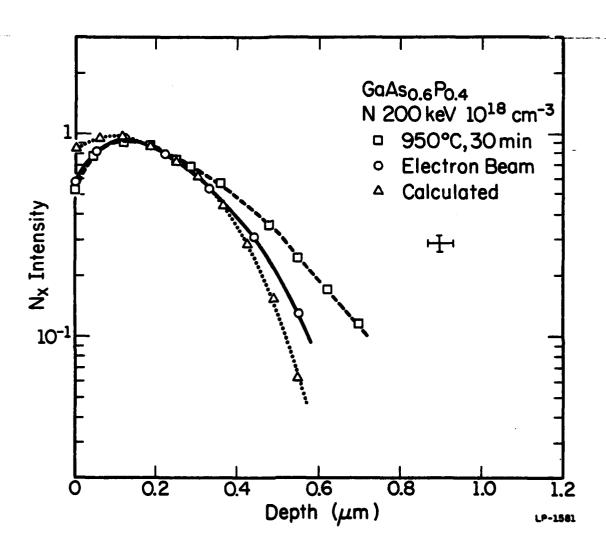


Fig. 5.3. Depth dependence of the N emission intensity (5°K) of GaAs 10.6°C.4 nitrogen implanted to a peak concentration of 10°C.4 cm. The dashed curve corresponds to furnace annealed material (950°C,30 min), and the solid curve to SLEB annealed material (I_b=12 mA, double pass). The theoretical emission profile (dotted line) is explained in the text. (After Yu |91|.)

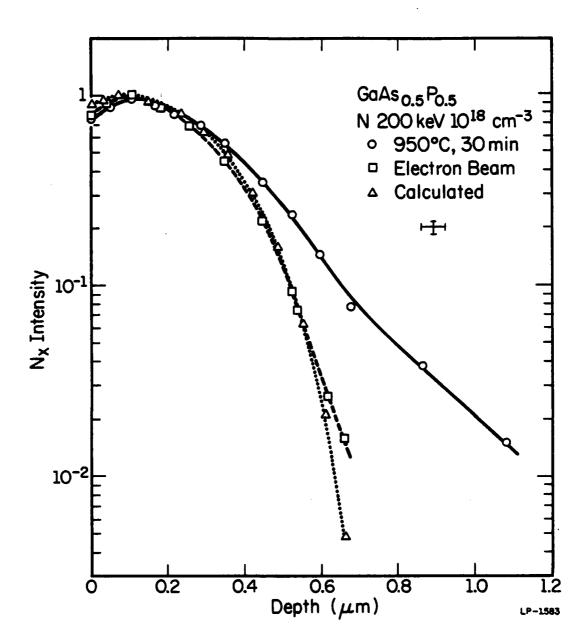


Fig 5.4. N_x emission intensity profiles as in fig. 5.3, for $GaAs_{0.5}^{P}O_{0.5}$ (indirect gap composition), nitrogen implanted to a peak concentration of 10^{18} cm⁻³. Notice the close agreement between the SLEB profile (I_b=12 mA, double pass) and the theoretical emission profile. Also notice the spreading of the furnace annealed profile. (After Yu | 91|.)

ference, we can unambiguously define the limit of nitrogen diffusion with the $N_{\rm H}$ profile. We estimate that the diffusive tails contain about 10% of the total implanted nitrogen for either composition.

5.2 Study of SLEB Annealed GaAs_{0.35}P_{0.65} p-n Junctions

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The study described in the preceding section shows the effectiveness of SLEB processing in activating N-implanted $GaAs_{1-x}^P$. However, in the case of x=0.65 composition material, migration of nitrogen and damage migration effects could not be verified. In addition, the N_x intensity profiles discussed above must rely upon a calculated excess carrier profile, rather than some more direct means. To investigate this particular composition further, a series of $GaAs_{0.35}^PO.65$ p-n junctions were fabricated which incorporated implanted nitrogen. The electrical and optical characteristics of these devices show that SLEB annealing does indeed reduce migration effects of implantation related damage and nitrogen when compared with conventional furnace annealing.

5.2.1 Experimental procedure

Material used in this portion of the study was indentical to the x=0.65 composition $GaAs_{1-x}P_x$ used for the photoluminescence experiments. As before, the 20 μ m nitrogen doped epitaxial layer was removed prior to processing. After cleaning, samples were subjected to two beryllium implantations of 1×10^{14} ions/cm² at 50 keV and 6.7 $\times 10^{14}$ ions/cm² at 130 keV. A single 3×10^{14} ions/cm², 220 keV nitrogen implantation was then made. The calculated as-implanted distributions are shown in figure 5.5. The Be doses and energies were chosen to produce the retrograde acceptor profile studied by Chatterjee.[113] This distribution was a compromise between a uniform and buried gaussian profile. The former

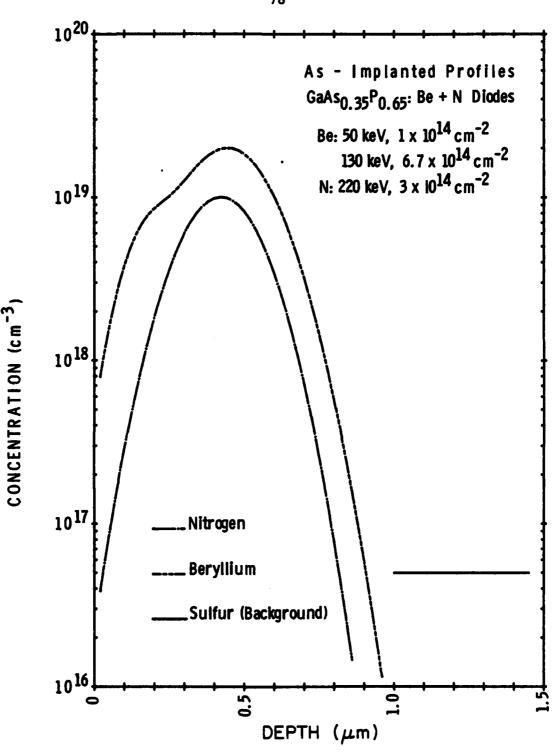


Fig. 5.5. Calculated as-implanted profiles of nitrogen and beryllium for the GaAs_{0.35}P_{0.65} p-n junctions. Also shown is the level of the substrate dopant concentration.

distribution simulates the zinc profile created in conventional furnace diffusion, whereas the latter produces a built-in retarding field for injected electrons, reducing surface recombination effects. Chatterjee's studies have suggested that the retrograde acceptor profile does indeed reduce surface recombination and results in the best light intensity (L) versus current characteristics among similar implanted direct-gap GaAsP light emitting diodes. The as-implanted nitrogen profile in figure 5.5 is entirely contained within the implanted acceptor profile.

Following implantation, samples were cleaned and encapsulated with ~ 1500 Å of rf plasma deposited silicon nitride.[114] Some of the material was then annealed in silica lined furnace tube under flowing high purity argon gas. A 30 minute, 950°C annealing cycle was selected, corresponding to the optimal conditions for annealing nitrogen implanted to this level.[91] Chatterjee[113] demonstrated successful annealing of Beimplanted direct gap GaAsP with these approximate implantation conditions at temperatures about 50°C less than used here. Samples for E-beam annealing were prepared as described in section 2.1. A table translation speed of 0.60 cm/sec was used for these samples. Although a number of different beam power density combinations were tried, the devices described here were processed with five passes of the SLEB with 18 W/cm² neak power density.

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Prior to annealing, all implanted samples possessed a frosted opaque appearance. After the first pass of the SLEB, the samples returned to their original orange transparent condition. This observation tends to indicate that good crystallinity had returned after this level of annealing. A survey of photoluminescence of this Be + N implanted material agreed with findings of section 5.1 In general, restoration of crystal order

occured after only a single pass of the SLEB, but complete nitrogen activation required more intense and repetitive E-beam treatment.

After annealing, samples were solvent cleaned and stripped of nitrides. Al contacts were then defined on the implanted surface by AZ photoresist lift-off technique. On the back surface, Au-Ge contacts were produced with Ni overlay by double evaporation through a shadow mask. The samples were then sintered in flowing H₂ for a total of approximately 90 secs. Maximum temperature reached during the contact processing did not exceed 400°C. Individual devices were formed by scribing and cleaving. Devices were mounted in pairs on TO-18 headers and thermocompression lead bonded.

5.2.2 Results and discussion: electrical characteristics

Current-voltage measurements were made on these devices with a computer controlled Hewlett Packard 69321 B power supply and a Keithley Model 480 Picoammeter. Temperature dependent measurements were made in a vacuum chamber equipped with an Air Products closed-cycle He refrigerator unit. Room temperature current density (J) versus voltage characteristics of the best furnace and SLEB annealed devices are shown in figure 5.6.

In the low forward bias region, both devices display conduction with an ideality factor n of 2. The furnace annealed device shows a marked departure from this behavior at $J=10^{-5}$ A/cm², and yet further bendover occurring at forward bias exceeding 2.5 volts. This departure from

^{*}n is the ideality factor commonly used in the diode expression $J = J_{q} \exp(qV/nkt)$

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(A)

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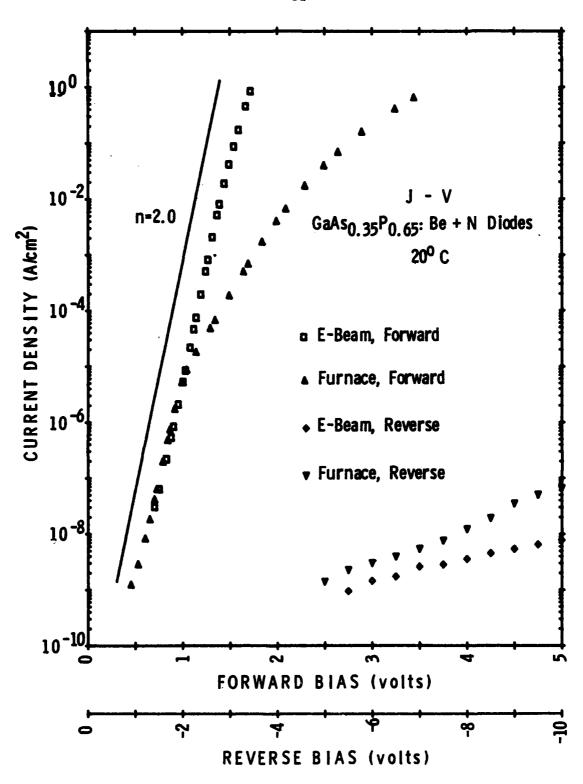


Fig. 5.6. Current density versus voltage characteristics for the best ${}^{GaAs}_{0.35}{}^{P}_{0.65}$:Be + N diodes annealed by SLEB and furnace techniques.

n=2 conduction occurs consistently for all 5 furnace processed devices between 10⁻⁵ and 10⁻⁶ A/cm². The e-beam device characteristic shows n=2 conduction nearly to the limit of current measurement. Some slight roll-off is seen at the highest measured currents, presumably due to series resistance effects. All but one of the eight beam processed devices show a predominance of current due to recombination in the space charge layer. The characteristics of the furnace annealed devices indicate the presence of series resistance in the junction.

Eliminating the worst device from each set, the average $V_r=10~V$ reverse current density is about $4\times10^{-7}~A/cm^2$ in the furnace annealed devices and $6\times10^{-8}~A/cm^2$ in the SLEB case. In general, the furnace annealed devices show a softer reverse bias characteristic.

Temperature dependent J-V data for devices T4B (furance) and E1B (SLEB) are presented in figures 5.7 and 5.8 respectively. Notice in figure 5.7 a set of parallel lines has been drawn through the approximate straight line portion of each curve, beginning just above the "knee" discussed earlier. The obvious temperature independence indicates conduction predominated by tunneling mechanisms.[115,116] One would therefore expect a relatively large number of states to be available within the bandgap at the n-type edge of the space charge region in these devices. The doping level of the substrate material is not sufficiently large to expect valence bandtail effects.[117] A similar set of parallel lines obviously cannot be drawn through the data of device E1B. Calculated ideality factors of the beam annealed device vary around 2 for all temperatures studied.

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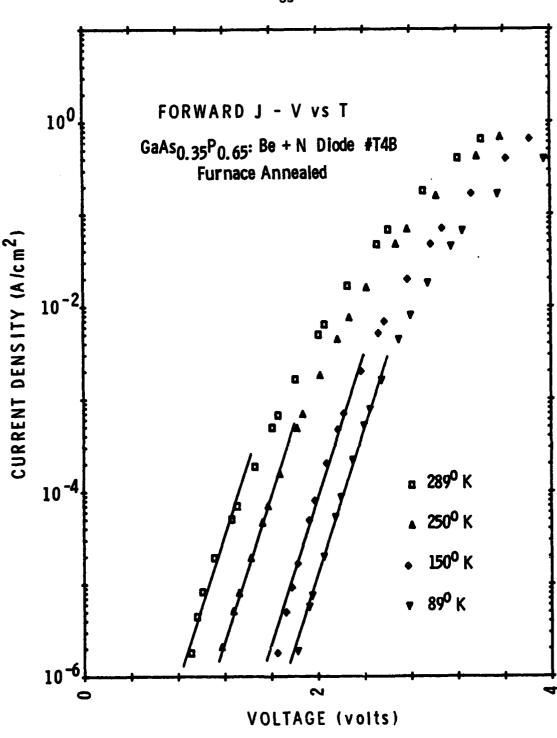


Fig. 5.7. Temperature dependent current density versus voltage characteristics for furnace annealed GaAs_{0.35}P_{0.65}:Be+N diode #T4B. The solid lines drawn through the low current density portion of each curve are exactly parallel to one another.

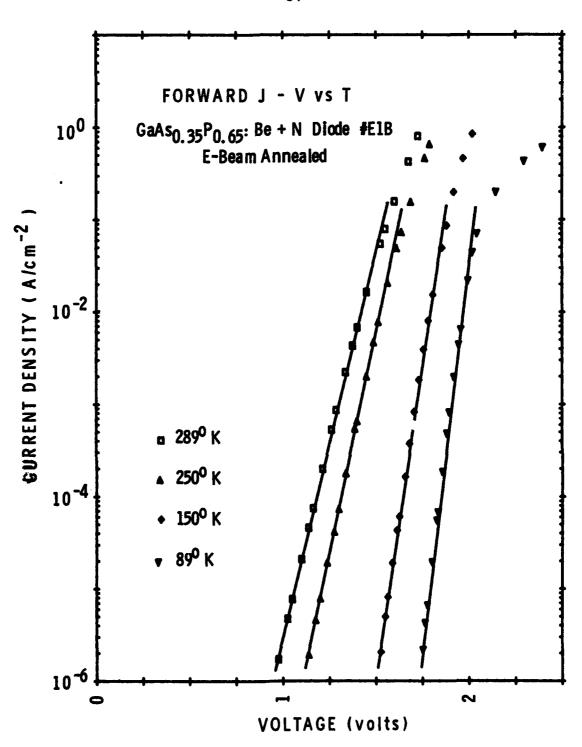


Fig. 5.8. Temperature dependent current density versus voltage characteristics for SLEB annealed device ElB. The solid lines drawn through each characteristic have ideality factors of about 2 at all temperatures. Note the shift in horizontal scale from figure 5.7.

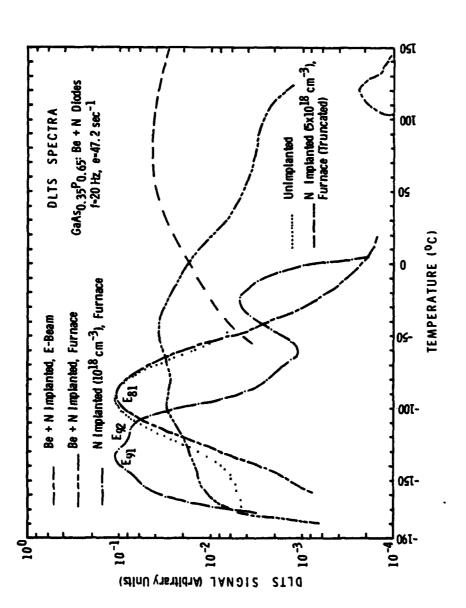
DLTS analysis tends to confirm these findings. The two-diode method described in section 2.3.2 is used. A survey of the electron trap spectra on the n-type side of the junctions of two representative devices is shown in figure 5.9. Here the SLEB and furnace annealed DLTS signal are plotted logarithmically in the same units. Quiescent reverse bias of -10 V and bias reducing pulses of +10 V were used for both devices. Corrections for device area are included so that the relative magnitudes of these curves are indicative of the relative trap densities between devices. Also plotted are survey spectra of Day[71] measured on Al Schottky barriers fabricated on material identical to that used in this study. These data were measured under identical frequency conditions, but not necessarily the same bias. Therefore for comparison, Day's data have been normalized to the peak value of the beam annealed sample's spectra.

The SLEB annealed sample shows a single large peak, while the furnace annealed device shows significant signal all across the scan. The defect spectra of the unimplated "nitrogen free" Schottky diode shows an amazing similarity to that of the beam annealed device. This defect (E₈₁, E=E_c-0.41 eV) has been associated with the dopant sulfur.[118] I conclude that these defects are intrinsic to the material and are not a product of the annealing. The average concentration of this trap can be estimated through [69]

$$N_{T}=2 \cdot (N_{d} - N_{a}) \cdot \Delta C/C$$
 (5.1)

to be about 1×10^{16} cm⁻³.

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DLTS spectra for GaAs_{0.35}P_{0.65}:Be+N diodes processed by SLEB and furnace annealing. Also shown are informalized spectra for unimplanted and N-implanted x=0.65 GaAs_{1-x}P_x Schottky barrier diodes as measured by Day et al. |71|. Note the logarithmic vertical scale. Fig 5.9.

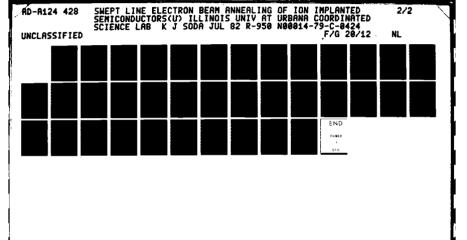
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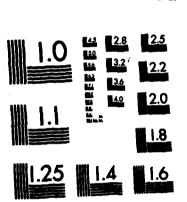
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The influence of trap signal E_{81} is apparent in the furnace annealed Re+N diode spectra at about $-95^{\circ}C$. This device also shows the effects of levels E_{91} and E_{92} observed in a nitrogen implanted Schottky diode.[71] Using equation 5.1 we may estimate the concentration of these defects to be about 2×10^{15} cm $^{-3}$. Although identification is not absolutely conclusive, it is probable that these signals are due to implanted nitrogen which as diffused out of the original implanted profile and beyond the metallurgical junction during furnace annealing.

Under similar implantation and furnace annealing conditions,
Chatterjee[113] found evidence of Be diffusion beyond the as-implanted
distribution. This has probably occured in the furnace annealed devices
under study here. They show consistently high voltage drops at large
forward currents. The average applied bias required for 10⁻¹ A/cm² current
density is 3.1 V for furnace annealed devices and only 1.5 V for SLEB
annealed devices. This tends to indicate a higher sheet resistance due
to spreading of the implanted profile. The nitrogen diffusion under consideration here must have proceeded at a faster rate than that of beryllium,
since it is detected in the space charge beyond the metallurgical junction.
It is significant that no nitrogen related signal is detected in the SLEB
annealed device. This coincides with the finding of the photoluminescence
study of section 5.1.

Also observed is a broad signal band in the furnace annealed Be + N diode spectra at temperatures above -50° C. Day[71] has found similar broad defect peaks in nitrogen implanted x=0.65 GaAs_{1-x}P_x. This is shown in the truncated 5 x 10^{18} cm⁻³ nitrogen implanted spectra cf figure 5.9. (This truncated curve is identical to the 10^{18} N-implanted spectra below -80° C.) It is significant to note that the SLEB annealed

device shows no similar radiation damage signal spectra, even though the material was implanted to a factor of two larger peak nitrogen concentration and was beryllium implanted as well. However, we cannot be completely certain that there are no hole traps in the depletion layer since hole injection was not performed during DLTS analysis.

Along this same line of argument, we may not conclude that the defects observed here are directly responsible for the modes of current conduction discussed above. Holes injected into the n-side of these devices will dominate conduction. However, it is interesting that, these furnace annealed Be + N diodes, which possess a continuum of deep levels, also demonstrate tunneling current components. As an order of magnitude estimate, if a 200 Å thick layer contained an average of 1 x 10^{15} traps/cm, each would need to recombine a hole-electron pair only once every 300 μ ses to support 10^{-6} A/cm² conduction. This is certainly not an unreasonably short lifetime.

5.2.3 Results and discussion: light emission characteristics

Although the principal purpose of these diodes was the study of redistribution phenomena by electrical techniques, their light emission characteristics also lend some support to the contentions of the preceding section. One would not expect large emission efficiencies in these devices. In this composition, GaAsP has an indirect gap, making bandedge radiative emission a low probability event. Nitrogen acts as an efficient isoelectronic trap of this composition, but the doping profile has not been optimized for maximum efficiency in these devices.

Light intensity (L) versus current data were taken by positioning the devices in a 180° polished aluminum reflector. This reflector was then attached to a Newport Model 880 radiometric detector system. The reflector/detector combination was designed to eliminate all background optical signals. Total optical power measurements were then made as a function of forward DC current. The data are corrected for photodetector response.

Two representative device characteristics are shown in figure 5.10. Shown for reference are lines indicating emission proportional to current density and to current density squared.

The slopes of the characteristics shown are representative of all devices annealed by the respective techniques. In general, furnace annealed diodes all show $L \propto J^{n>1}$ behavior while all SLEB annealed devices show $L \propto J^{n\sim 1}$. This trend indicates that some space charge recombination current is contributing to the emission of the furnace annealed diodes, while diffusion current related emission dominates in the SLEB annealed case. [113] This finding is not inconsistent with the J-V measurements discussed earlier. Ohmic losses are considerable at the current densities—where light intensity is large enough to measure. Therefore, we are not able to identify the dominant mode of conduction at these current levels. The average external quantum efficiency for the furnace annealed devices is about 5 x 10^{-6} photons/electron for the furnace annealed diodes and about 2.8×10^{-6} for SLEB annealed devices. A figure of about 2×10^{-5} is expected from published results in furnace diffused x=0.65 LEDs without nitrogen doping. [119]

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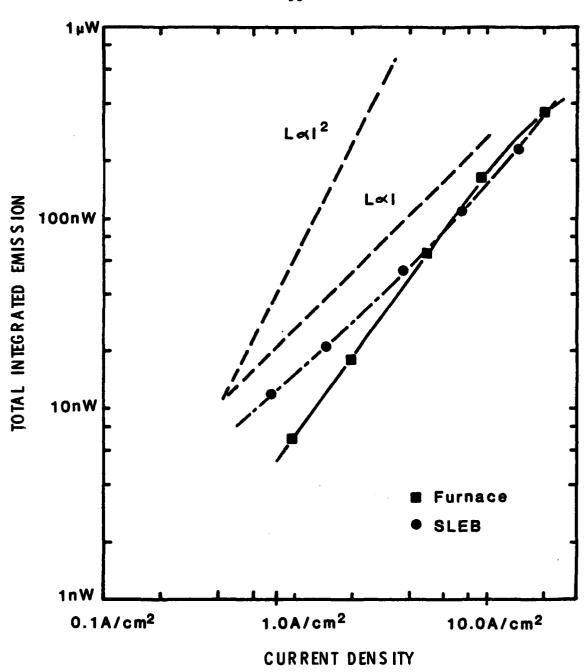


Fig 5.10. Total integrated electroluminescent emission versus current density for representative SLEB and furnace annealed $GaAs_{0.35}^{P}_{0.65}^{:Be+N}$ diodes. Also shown are lines indicating L α I and L α I emission dependence.

Since nitrogen is known to exist in the space charge region of the furnace treated devices, one might expect that some isoelectronic trap emission might be observed. This occurs to some extent. The detection system described in section 5.1 was used to make electroluminescence measurements. The peak emission wavelength of the beam annealed device E1A 6018 Å (2.060 eV), is consistent with that expected from measurements of Crawford et al. [120] for GaAsP without nitrogen doping. Very little current dependent emission shift is observed in this device from 17 to 40 A/cm². Peak emission for the furnace annealed device T4A is nearly identical to E1A at low bias, but shifts over 70 Å to 6078 Å (2.040 eV) at 25 A/cm². This wavelength corresponds roughly with the expected N_X (A-line) nitrogen emission. [120]

The results sugggest again that some depletion region nitrogen involvement occurs in the case of the furnace annealed devices. It is possible that the nitrogen related emission also has some component from electrons injected into the p-side of the junction. The reduced doping gradient expected in the furnace annealed case would allow increased electron injection efficiency. The current dependence of the emission tends to confirm this proposition.

5.3 Summary and Conclusions

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In this chapter it was demonstrated that SLEB annealing is effective in activating ion-implanted nitrogen in both direct and indirect gap composition $GaAs_{1-x}^{P}_{x}$. Photoluminescence analysis shows that under some conditions nitrogen related emission can actually exceed that attainable by furnace annealing. Photoluminescence profiling demonstrates that SLEB annealing is also effective in restricting the migration of nitrogen and ion-implantation related damage to the original implanted layer.

Although this technique could not be used to verify this finding in x=0.65 composition material, electrical studies of Be + N implanted diodes do tend to confirm this finding. J-V, DLTS, L-J, and spectral emission characteristics all can be understood in terms of restricted motion of nitrogen and related damage during annealing. These data also show a lack of Be migration in SLEB treated devices, in contrast with the furnace annealed case.

CHAPTER 6 - SUMMARY AND RECOMMENDATIONS

In this study, the behavior of swept-line electron beam (SLEB) annealed, ion-implanted semiconductors has been studied in some detail. In general it is found that SLEB processing can be an effective and practical alternative to furnace annealing. SLEB treatment has been shown to be effective in annealing implantation related damage in silicon, especially in the as-implanted amorphous-crystalline transition region. This transition region damage has been shown to be resistant even to high temperature furnace annealing, and can act to skew dopant distributions through damage aided diffusion. These migration effects are much less pronounced in SLEB annealed amorphous silicon. SLEB induced activation of boron in this transition region has also been demonstrated. This has not been observed in furnace annealed silicon.

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The success of this annealing technique is not limited to silicon. Photoluminescence studies have shown the effectiveness of the SLEB technique in activating implanted nitrogen in $GaAs_{1-x}^{P}_{x}$. In some cases, nitrogen isoelectronic trap related emission intensities are actually larger than those observed from similarly prepared furnace annealed material. Photoluminescence profiling and p-n junction studies show that SLEB annealed material does not display dopant and implantation damage migration effects present in optimally prepared furnace annealed material.

Although this study demonstrates that SLEB annealing is an effective processing technique, a number of questions remain to be answered. The possibility of upscaling a line beam to treat industrial-size wafers was not completely investigated. A prototype electron gun with a four inch beam was built but could not be completely developed.

As designed, however, it meets the criteria observed to be necessary

for successful large scale applications. First, it does not rely upon overlap of annealed areas, but rather treats large substrates in a single pass. Experiments with the electron gun described in chapter 2 show that stress marks develop on material adjacent to the beam track on wafers larger than the beam spot. No such stressing appear within the beam heated regions. Also, the long-line gun will deliver all of its energy in a thin (10 mil) line. This should improve annealing uniformity, especially on samples which are non-rectangular. If the sample is heated only within a thin line and is translated fast enough, significant lateral heat flow will not occur. This should limit hot spots on the substrates which occur when broader beam shapes are used.

The results discussed here represent only a relatively limited portion of the range of annealing parameters possible. The fact that annealing quality can exceed that achievable by conventional annealing should stimulate further study. The question of the exact process by which point defects are annealed has not been adequately answered. The degree of permanence of this annealing is unknown. Electric field dependent aging studies of SLEB annealed devices would be a useful investigation. Some obvious differences in the annealing conditions optimal for different semiconductors were noted during these studies. For example, multi-pass annealing depresses the active boron profiles in implanted Si, while it works quite well in implanted GaAsP. The electron range and implantation and damage distributions all undoubtedly affect the ultimate quality of treatment. Some theoretical treatment of beammaterial interaction could lead to more predictable processing.

APPENDIX

TRAPSI PROGRAM DOCUMENTATION

TRAPSI is a FORTRAN program for computing defect depth profiles from DLTS measurements at fixed reverse bias and varying bias reducing pulse height. This program is designed for analysis of Schottky barriers fabricated on n-type silicon. Modifications can easily be made for other semiconductor materials. The general operating principles of TRAPSI were described in section 2.3.2.2. The appendix includes specific input requirements, a block by block description of operation, a copy of the program, and a sample output.

A.1 Input Requirements

1

The TRAPSI program requires three data types: (i) that which relates to the device in general; (ii) C(V) data for determination of fixed charge concentration; and (iii) the DLTS data relative to the defect level in question. Data may be entered indefinitely so that defect peaks of different activation energy and from different devices may be analyzed without restarting the program.

Immediately after execution, the program asks for type i data through the interactive terminal (#5). The data are: (The FORTRAN variable is listed after each entry.)

- a. Descriptive one line comment.
- b. Device area in cm² (AREA).
- c. Relative dielectric constant for the semiconductor (ER).

 The static value may be used with confidence for Si, Ge and GaAs. Other

values may be more applicable for materials with relatively large dielectric relaxation times [121]

- d. Metal-semiconductor barrier height in volts (DPHIBN).
- e. Density of states effective mass for electrons (MDEE) and holes (MDEH).
 - f. Donor activation energy in electron volts. (EDON).

The program then asks for the file name which contains the C(V) data (type ii) for the device in question. This file must contain two columns of data, the left hand containing the capacitance in pf, the right hand the corresponding voltage in volts. Up to 100 data pairs may be entered. The last pair of data points in the file must both be zero. All negative voltages should be entered as negative numbers. All effective bias voltages and corresponding steady state capacitances used in the DLTS profiles should be included in this list. All static capacitance data are automatically reduced by 0.68 pf, the average parallel capacitance of a TO-18 header.

Since the fixed charge concentration is inversely proportional to dC/dV, it is important that enough static capacitance data be entered to produce good estimates of $N_d(x)$. The program has an internal criterion that dC/dV be calculated from capacitance values which differ by at least 1% and no more than 10% of the capacitance in question. If this criterion is not met, an error flag appears on the far left side of the output. C(V) data may be entered either largest or smallest value first, but must increase or decrease continuously.

The defect peak related data (tyve iii) are then entered. They are:

- a. Descriptive comment relative to this defect.
- b. Value of fixed DC reverse bias maintained during profiling, in volts. (VBIAS).
- c. The temperature in ^OK at which the peak trap signal occurs (TEMP).
 - d. Total number of DLTS data points (CPTS).
- e. The value of the bias reducing puls height in volts (VR), the peak recorder displacement in cm (DISP(I)), the sensitivity of the lock-in amplifier in volts (S(I)), and the calibration factor in V/pf (CVF(I)).

The program will ask for data of type e repetitively until the total number of transient points (CPTS) have been recieved. After the last entry, the program will ask if another defect peak is to be analyzed. If so, it will ask for new type iii data. If not, another device may be analyzed by supplying new type i and ii data. A sample interactive output is shown on the following two pages. Entries made by the operator are underlined.

A.2 Block Description

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A description of TRAPSI code is presented in this section. The line numbers found at the beginning of each entry correspond to these generated by the DEC FORTRAN editor as shown on the program listing found in section A.3.

Line 100-900: Descriptive comments.

Line 1000-1700: Variable, array and type declaration.

Line 1800-5200: Entry of type i data.

Line 5300-6900: Entry of file name containing C(V) data arrays

```
EXECUTE TRAPSI.FOR
 LINK: Loading
CLNKXCT TRAPSI execution]
ENTER ONE LINE COMMENT
 FROFILE FOR E BEAM S. B. $31A
ENTER DEVICE AREA (CM**2) - 1.32E-3
ENTER RELATIVE DIELECTRIC CONST. -
 ENTER DELTA PHI B-N (VOLTS)=0.7
DENSITY OF STATES EFFECTIVE MASSES OF COMMON
 SEMICONDUCTORS:
                      ELECTRONS HOLES
 SI
                                        .55
                           1.1
 GAAS
                            .068
                                        ٠5
 GAASP 40%
                            .089
 GAASP INDIRECT
                           1.20
                                        . 5
                          1.20
                                        . 5
 MDE FOR ELECTRONS=1.1
 MDE FOR HOLES=.55
DONOR ACTIVATION ENERGY (EV)=0.044
 ENTER NAKE OF C(V) DATA FILE: DEB31A
 C(V) DATA READ A-OK
 ENTER 1 LINE COMMENT
PEAK I -- 0.32 EV
VALUE OF DC BIAS (VOLTS)=-10.00
ENIER TEMP OF PEAK(DEG K) 183.50
ENTER DELTA CAP DATA. # OF PTS=4
BIAS REDUCTING PULSE(VOLTS) V( 1)=10.5
ENTER VAL # 1 OF DISP (CM), SENS. (V), CONVER. FACT. (V/PF)
VALUE # 10-
                        <u>. 567</u>
             10F PULSE=
                                  10.50000
  OF DISP=
OF SENS=
                8.02000
                   0.02000
OF CON. FACT.= 0.36700

OK? -- 1=YES,0=NO: 1

BIAS REDUCTING PULSE(VOLTS) V( 2)=10.00
FHTER VAL $ 2 OF DISP (CM), SENS. (V), CONVER. FACT. (V/PF)
8.19 .020 .530
VALUE $ 20F PULSE=
                                   10.00000
 OF DISP=
OF SENS-
               8.19000
0.02000
 OF CON. FACT.= 0.53000

OK7 -- 1=YES,0=NO: 1

7 0.500 1.23290E+02
                                                6.99860E-02
                                                                          2.94509E-02
                                                                                                 -6.24272E-04
2.02015E-06 2.29572E+17
BIAS REDUCTING PULSE(VOLTS) V( 3)-6.50
                                                       3.71246E+12
ENTER VAL # 3 OF DISP (Ch), SENS. (V), CONVER. FACT. (U/PF)
8.27
VALUE $ 30F PULSE:
                                    4.50000
 OF DISP= 8.27000
OF SERR= 0.02000
                   0.02000
 OF CON. FACT.=
                          0.54200
 067 -- 1=YES+0=NO: 0
BIAS REDUCTING PULSE(VOLTS) V( 3)=9.5
ENTER VAL * 3 OF DISP (CM). SENS. (V), CONVER. FACT. (V/PF)
```

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```
8.27 .020
VALUE # 30F PULSE=
                                       9.50000
OF DISP= 8.27000

OF SENS= 0.02000

OF CON. FACT.= 0.00000

OK? -- 1=YES,0=NO: 0

BIAS REDUCTING PULSE(VOLTS) V( 3)=9.5

ENTER VAL $ 3 OF DISP (CM), SENS. (V), CONVER. FACT. (V/PF)
8.27 .020 .542
VALUE # 30F PULSE=
OF DISP= 8.27000
OF SENS- 0.02000
                                       9,50000
  OF CON. FACT. = 0.54200
OK? -- 1=YES.0=NO: 1
       0.000 1.00880E+02 9.24775E-02
9.67390E-06 4.28562E+16 6.76468E+12
                                                                                3.8482GE-02
                                                                                                             -2.65722E-04
BIAS REDUCTING PULSE(VOLTS) V( 4)=9.0
FNTER VAL 4 4 OF DISP (CM), SENS. (V), CONVER. FACT. (V/PF)
8.19 .020 .545

VALUE * 40F PULSE=

0F DISP= 8.19000

0F SENS= 0.02000
                                        9.00000
 GR? -- 1=YES.0=NO: 1
                                                         .....72E-02 4.34221E-03
1.31186E+13
7.36192E-02
 0 -0.500 7.32700E+01 9.36192E-02
1.51893E-05 3.92206E+16 1.31186E
0 -1.000 6.04500E+01 9.36192E-02
1.94826E-05 3.92578E+16 3.27133E
                                                                                                               2.28399E-04
                                                                                                             -3.45861E-03
                                                         3.27133E+14
IS THERE ANOTHER TRAP PEAK FOR THIS DEVICE?
1=YES+0-NO
THE YOU WISH TO ANALYSE ANOTHER DEVICE?
1=YES, 0-NO
Ç
END OF EXECUTION
CPU TIME: 1.96 ELAPSED TIME: 4:21.17
EXIT
```

(CCV(I) and VCV(I)). Included are checks for end of file (line 6000), correction for parallel header capacitance (6300) and file overflow (6600).

Line 7000-7900: Entry of DLTS defect peak related comment.

Line 8000-9100: Entry of quiescent DC reverse bias (VBIAS) and search of corresponding value of static capacitance (CBIAS). If the search fails to find a VCV(I)=VBIAS, then CCV(2)=CBIAS.

Line 9200-10000: Entry of defect peak temperature (TEMP) and number of transient capacitance points. N_c , N_v , and E_g are calculated in the block.

Line 10100-10400: Initialize profile calculation accumulators.

Line 10500: Initialize the main DO loop for profile calculation.

Line 10600-10700: Reset dC/dV flags. (F, F1)

Line 19800: Test for I=CPTS+1. If true, programs skips over transient capacitance data input steps. Note that DLTS data are received only when 1<1<CPTS, and values of trap concentration are calculated only when 2< I<CPTS+1.

Line 10900-12300: Input and confirm values for the type iiie.

(VR, DISP(I), S(I), CVF(I)). Largest values of bias reducing pulse (VR)

must be entered first. Allowance is made to correct data if miskeyed.

Effective bias (VDELC(I)) is calculated in line 11200.

Line 12400: Calculate Ith value of $\Delta C/C$ (DELCT(I)).

Line 12500: If I=1, VDLEC(0)=VBIAS. This step allows calculation of the fixed charge concentration (NB(1)) at the depletion depth corresponding to VBIAS.

Line 21600-13600: Search for the value of VCV(J) which equals VDELC(I-1). If the search fails, the flag Fl is set and the next closest

value of VCV is selected. If the selected value is the first or last in the array, the next value down or up the list is selected. This allows calculation of dC/dV.

Line 13700-15500: Search of the array CCV(I). Beginning with the Jth value selected in the previous block, values of CCV are identified which are at least 1% but not more than 10% different from the Jth value. If the search does not find values to fit this criteria, flag F is set and first CCV value is selected which is at least 1% different from the Jth value. These are designated CCV(U) and CCV(L).

Line 15600-15900: Values of dC/dV (DCDV) and fixed charge concentration (NB(I-1)) are calculated. Note that during each iteration, the I-1 value of NB and NT are calculated.

Line 16000-16300: Debugging print statements for NB and related variables. These lines may be deleted if desired.

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Line 16400: In the case I=1, skip the blocks concerning trap concentration calculation.

Line 16500-19700: Calculate the location of the Fermi level.

This is accomplished by solving the transcendental equation:

 $N_c \exp(-(E_c - E_v)/kT) = N_d/1 + 2 \exp(-(E_f - E_d)/kT) + N_v \exp(-(E_v - E_f)/kT)$ A.1 The value of E_f is systematically varied until the difference between left and right hand sides of equation A.1 is less than 0.01% of E_g , of until 50 iterations are completed. In the latter case, an error message (line 19200) is printed and the program continues.

Line 19800-21800: This block calculates the depletion width W(I). A basic derivation of the expression used is given here. We begin

with the expression for depletion width for a Schottky barrier:

$$\frac{\varepsilon_r \varepsilon_o}{q} (V_{bi} - \frac{kT}{q} - V) = \int_0^W x N_b(x) dx$$
 A.2

where

$$V_{bi} = \phi_{bn} + \Delta \phi - (E_c - E_f)/q \qquad A.3$$

Here V_{bi} is the built-in voltage, V is the applied bias, ϕ_{bn} is the Schottky barrier height, $\Delta \phi$ is the image force barrier lowering, N_b is the background fixed charge concentration. We may generalize this equation to:

$$\frac{\varepsilon_{\mathbf{r}} \varepsilon_{\mathbf{o}}}{q} (\mathbf{v}_{\mathbf{b}i} - \frac{\mathbf{k}\mathbf{T}}{q} - \mathbf{v}_{\mathbf{j}}) = \sum_{i=1}^{k} \mathbf{w}_{i} \mathbf{N}_{\mathbf{b}} (\mathbf{v}_{i}) [\mathbf{w}_{i} - \mathbf{w}_{i-1}]$$
 A.4

liml + o

where $N_b(V_i)$ is the background fixed charge concentration at the depletion depth corresponding to V_i . If we let $(\varepsilon_r \varepsilon_o)/q = b$ and $V_{bi} - (kT/q) - V_j = v_n$, we may write:

$$bv_1 = N_b(V_1) W_1^2$$

$$A.5$$

$$bv_2 = N_b(V_1) W_1^2 + N_b(V_2) [W_2^2 - W_2W_1]$$

$$bv_n = N_b(v_1)w_1^2 + \dots + N_b(v_n) [w_n^2 - w_n w_{n-1}]$$

Substracting the last two lines we have:

$$bv_{n} - bv_{n-1} = N_{b}(v_{n}) [w_{n}^{2} - w_{n-1}w_{n}]$$
 A.6

which may be solved quadratically for W if W and N $_b(v_n)$ are known. W is given by the first of equations A.5. This scheme is implemented in

lines 20100 through 20600. v_i is calculated in line 20000. In order to obtain the best estimate of W, $\Delta\phi$ is calculated iteratively (DO loop line 19900) based upon the latest value of W_n using:

$$\Delta \phi_{i} = \sqrt{\frac{qE}{4\pi\epsilon_{o}\epsilon_{r}}} = \left(\frac{q^{2}}{4\pi\epsilon_{o}^{2}\epsilon_{r}^{2}}\right)^{\frac{i-1}{2}} \left[\sum_{j=1}^{2} \left\{N_{b}(V_{j})W_{j} + N_{b}(V_{j})(W_{j} - W_{j-1})\right\}\right]^{1/2} A.8$$

New values of W_n are found based upon this value of $\Delta\phi_i$. This processes continues until the difference between successive calculations of W_n is less than 10^{-9} cm. We assign the term in brackets the label ACCDPT. The value of ACCDPT is accumulated for the next profile step in the variable ADDCP. Print statements 21300-21600 were for debugging and are not active.

Line 21900-22300: Calculate average value of $\delta(\Delta C/C)$ (DELC(I-1). The I-2, I-1 and Ith values of DELC and VDELC are used. If I=2 or CPTS+1, only the I-1 and CPTS values of DELC and VDELC respectively are used.

Line 22400: Calculate trap concentration. See section 2.3.2.2. Line 22500-23500: Print results of this profile step.

Line 23600-27700: Termination steps. The program asks if additional profiles or other devices are to be analyzed. If so, execution returns to lines 7000 and 1800 respectively.

This program was specifically written for silicon Schottky barriers. Modification for other semiconductor types requires (1) replacement of line 9700 with an expression to calculate $\mathbf{E}_{\mathbf{g}}$ as a function of temperature

and (2) inclusion of ϵ_r in the calculation of $\Delta \phi$ in line 21200. Conversion for p-type semiconductors will require further modest modification.

A.3 TRAPSI Code and Sample Output

A copy of the TRAPSI code and a sample output follow. The sample output corresponds to the example interactive output found in section A.1.

```
00100
                 TRAPSI.
        C
00200
        C
00300
        C
00400
        C
                 THIS PROGRAM COMPUTES TRAP DEPTH PROFILES FROM A
00500
        C
                 SERIES OF DLTS SCANS OF VARYING BIAS REDUCTING
00600
        C
                 PULSE HEIGHTS. PROGRAM IS DESIGNED FOR S.B. ON
        C
00700
                 N-TYPE MATERIAL. PROGRAM COMPUTES DEPLEATION
00800
                 WIDTH FROM FIXED CAPACITANCE DATA WHICH YOU
00900
                 MUST PROVIDE. THIS VERSION READS C(V) DATA FROM A DISK FILE.
01000
                 REAL S(50), CVF(50), DISP(50)
01100
                 REAL DELC(50), DELCT(50), VB(50), W(0:50)
01200
                 REAL AREA, ER, MDEE, MDEH, EGEF, VBIAS, CBIAS, VR
01300
                 REAL MI, NC, NV, EG, EF, EFDIFF, INC, EDONN, DELPHI, DPHIBN, WOLD
01400
                 REAL ACCOP, DCDV, CTEMP, PT1, PT2, PT3, ACCOPT
01500
                 REAL A(90),NT(50),NB(0:50),CCV(100),VCV(100),VDELC(50)
01600
                 INTEGER CPTS, F, F1, J, K, I, U, L, Q, X, N, F2, NPOINT, O, T
01700
                 DOUBLE PRECISION B
                 WRITE(5, 10)
01800
                 FORMAT(1X, ENTER ONE LINE COMMENT ,/)
READ(5,20) A
01900
         10
02000
02100
                 FORMAT (SOA1)
         20
02200
                 PRINT 30, A
                 FORMAT (1X, 80A1)
02300
         30
02400
                 WRITE(5,40)
                 FORMAT(1X, ENTER DEVICE AREA (CM**2) - .$)
02500
         40
02600
                 READ(5,50) AREA
02700
         50
                 FORMAT(G)
02800
                 WRITE(5,60)
02900
         60
                 FORMAT(1X, ENTER RELATIVE DIELECTRIC CONST.
03000
                 READ(5,50) ER
03100
                 WRITE(5,65)
03200
         55
                 FORMAT(1X, ENTER DELTA PHI B-N (VOLTS)= ',$)
03300
                 READ(5,50) DPHIBN
03400
                 WRITE(5,70)
03500
         70
                 FORMAT(1X, DENSITY OF STATES EFFECTIVE MASSES OF COMMON /
              C
03600
                   SEMICONDUCTORS: 1/
              C
03700
                                    ELECTRONS
                                                HOLES /
                 SI
              C
                                                 .551/
03800
                                       1.1
03900
              C
                   GAAS
                                                 .51/
                                        -068
04000
              C
                   GAASP 40%
                                                 .51
                                        .039
                  GAASP INDIRECT
04100
                                       1.20
                                                 .51
                 GAP
04200
                                       1.20
                                                 .51/)
                 WRITE(5,80)
04300
04400
                 FORMAT(1X. MDE FOR ELECTRONS=1.$)
         90
04500
                 READ(5.50) MDEE
04600
                 WRITE(5,90)
                 FORMAT(1X, MDE FOR HOLES=*,$)
READ(5,50) MDEH
04700
04800
04900
                  WRITE(5,91)
                  FORMAT(1X, DONOR ACTIVATION ENERGY (EV)= 7,8)
05000
         91
05100
                  READ(5,50) EDON
05200
                  WRITE(5, 100)
                  FORMAT(1X, ENTER NAME OF C(V) DATA FILE: 7,5)
05300
         100
05400
                  READ(5,105) B
```

C

```
05500
         105
                  FORMAT(A9)
05600
                  OPEN (UNIT=20, DEVICE='DSK', ACCESS='SEQIN', FILE=B)
05700
                  DO 130 I=1,100
                  READ(20,110) CTEMP, VCV(I)
05800
05900
         110
                  FORMAT(2G)
06000
                  IF (CTEMP.EQ.O. AND. VCV(I).EQ.O) 120.125
06100
         120
                  NPOINT=I-1
06200
                  GO TO 138
                  CCV(I)=CTEMP-0.68
06300
         125
06400
         130
                  CONTINUE
06500
                  WRITE(5, 131)
06600
                  FORMAT(1X. C(V) DATA FILE TOO LARGE -- CONTINUING ANYWAY ./)
         131
06700
                  GO TO 140
06800
         138
                  WRITE(5, 139)
06900
                  FORMAT(1X, C(V) DATA READ A-OK ,/)
         139
07000
                  WRITE(5,141)
         140
07100
         141
                  FORMAT(1X, ENTER 1 LINE COMMENT,/)
07200
                  READ(5,20) A
07300
                  PRINT 30, A
07400
                  PRINT 145
                  FORMAT(2X, F, 3X, V-REV, 8X, S.S. CAP, 10X, EC-EF,
07500
         145
                  12X, DELPHI, 7X, AVG. D(DC/C)/DV, 4X, DEP. WIDTH,
07600
                 5X, DOPANT CONCNT. ,5X, TRAP CONCNT. ,/,5X, (VOLTS),
9X, (PF) ,12X, (EV) ,13X, (VOLTS) ,9X, (1/VOLTS),
9X, (CM) ,12X, (CM**-3) ,10X, (CM**-3))
07700
07800
07900
08000
                  WRITE(5, 150)
                  FORMAT(1X, VALUE OF DC BIAS (VOLTS)= ',$)
READ(5,50) VBIAS
081 00
         150
08200
08300
                  DO 160 I=1, NPOINT
09400
                  IF (VBIAS.EQ.VCV(I)) GO TO 180
08500
         160
                  CONTINUE
08600
                  WRITE(5, 170)
08700
         170
                  FORMAT(1X, VBIAS=VCV(I) NOT FOUND. C(VBIAS) SET TO C(2),/)
08800
                  PRINT 170
                  CBIAS=CCV(2)
08900
09000
                  GO TO 181
091 00
         180
                  CBIAS=CCV(I)
09200
                  WRITE(5, 190)
         181
09300
                  FORMAT(1X, ENTER TEMP OF PEAK(DEG K) ',$)
READ(5,50) TEMP
         190
09400
09500
                  NC =4.8290E15*MDEE**1.5*TEMP**1.5
                  NV =4.8290E15#MDEH##1.5#TEMP##1.5
09600
09700
                  EG=1.16-(7.02E-4*TEMP**2)/(1108+TEMP)
09800
         200
                  WRITE(5,210)
                  FORMAT(1X, ENTER DELTA CAP DATA. # OF PTS=1,8)
09900
         210
10000
                  READ(5,50) CPTS
10100
                  WOLD=0.001E-5
10200
                  ACCDP=0
10300
                  ACCDPT-0.0
10400
                  W(0)=0
10500
                   DO 510 I=1,CPTS+1
10600
                  F=0
10700
                  F1=0
10800
                   IF (I.EQ.CPTS+1) GO TO 245
         219
10900
                  WRITE(5,220) I
```

```
FORMAT(1X, BIAS REDUCTING PULSE(VOLTS) V('.13.')='.$)
11000
        220
11100
                 READ(5.50) VR
11200
                  VDELC(I)=VBIAS+VR
11300
                  WRITE(5,230) I
                 FORMAT(1X, ENTER VAL #,13, OF DISP (CM), SENS. (V), CONVER. FACT. (V/PF),/)
11400
         230
11500
11600
                  READ(5,240) DISP(I),S(I),CVF(I)
117CO
         240
                  FORMAT(3(G))
                  WRITE(5,235) I, VR, DISP(I), S(I), CVF(I)
11800
                  FORMAT(1X, VALUE # ,13, OF PULSE= ,F12.5,/, OF DISP= ,F12.5,/, OF SENS= ,F12.5,/, OF CON. FACT.= ,F12.5,/,
11900
         235
12000
12100
                     OK? -- 1 = YES, O = NO: (,$)
12200
                  READ (5,50) T
12300
                  IF (T.EQ.O) GO TO 219
                  DELCT(I)=(S(I)*DISP(I)*.5650*.5)/(CVF(I)*CBIAS)
12400
                  IF (I.EQ.1) VDELC(O)=VBIAS
12500
12600
         245
                  DO 250 J=1, NPOINT
                  IF (ABS(VDELC(I-1)-VCV(J)).LE.1E-5) GO TO 260
12700
                  CONTINUE
12800
         250
                  F1=1
12900
13000
                  MI=VDELC(I-1)
13100
                  DO 255 J=1.NPOINT
13200
                  IF (ABS(VDELC(I-1)-VCV(J)).LT.MI) 253,255
13300
         253
                  MI=ABS(VDELC(I-1)-VCV(J))
13400
                  Q=J
13500
         255
                  CONTINUE
13600
                  IF (Q.EQ.NPOINT) J=Q-1
13700
                  IF (2.EQ.1) J=2
13800
         260
                  DO 270 K=1, NPOINT
                  IF (K+J.EQ.NPOINT) GO TO 280
13900
                  IF (ABS(CCV(K+J)-CCV(J)).GT.(0.01*CCV(J))) GO TO 290
14000
         270
                  CONTINUE
14100
14200
         280
                  U=K+J
14300
                  F=1
14400
                  GO TO 310
14500
         290
                  IF (ABS(CCV(K+J)-CCV(J)).LE.(0.1*CCV(J))) 300,280
14600
         300
                  U=K+J
                  DO 320 K=1, NPOINT
         310
14700
                  IF (J-K.EQ.1) GO TO 330
14800
14900
                  IF (ABS(CCV(J-K)-CCV(J)).GT.(0.01*CCV(J))) GO TO 340
15000
         320
                  CONTINUE
15100
         330
                  L=J-K
                  P=1
15200
                  GO TO 360
15300
                  IF (ABS(CCV(J-K)-CCV(J)).LE.(0.1*CCV(J))) 350,330
15400
         340
15500
         350
                  L=J-K
15600
         360
                  DCDV = ((ABS(CCV(IJ)-CCV(J)))/(ABS(VCV(U)-VCV(J)))+
                  (ABS(CCV(J)-CCV(L)))/(ABS(VCV(J)-VCV(L))))/2
15700
15800
                  NB(I-1)=CCV(J)**3/(1.418E-9*ER*AREA**2*DCDV)
15900
                  IF (NB(I-1).LT.O) NB(I-1)=ABS(NB(I-1))
                  PRINT 361, NB(I=1), DC DV, CCV(J), CCV(U), CCV(L)
16000
         362
                  WRITE (5,361) NB(I-1), DCDV, CCV(J), CCV(U), CCV(L)
16100
                 FORMAT( NB(I-1)= ,1PE11.3, DCDV= ,1PE11.3, 2PE11.3, CCV(U)= ,2PE11.3, CCV(L)= ,2PE11.3)
                                                                         CCV(J)=1
         361
16200
16300
16400
                   IF (I.EQ.1) GO TO 510
```

```
16500
         363
                  INC =O. 10 EG
16600
                  F2=1
16700
                  EF-0.50*EG
                  DO 390 0=1,50
16800
16900
                  PT1=EXP(-1.0*(EG-EF)/(8.6171E-5*TEMP))
17000
                  PT 2=NB(I-1)/NC
                  PT 3=(1.0/(1.0+2.0*(EXP((EF-EG+EDON)/(8.6171E-5*TEMP)))))
17100
                  EFDIFF=PT1-PT2*PT3
17200
                  IF (0.EQ.1) GO TO 355
17300
17400
                  GO TO 365
17500
         355
                  SIGN=EFDIFF
17600
                  GO TO 385
17700
         365
                  IF (F2.EQ.1) 370,380
17800
         370
                  IF ((SIGN.LT.O.AND.EFDIFF.GT.O).OR.(SIGN.GT.O.AND.EFDIFF.
17900
               C LT.O)) 371,372
18000
         371
                  F2=-1
18100
                  SIGN-EFDIFF
18200
                  INC =O.1 FINC
18500
                  GO TO 372
18400
         380
                  IF ((SIGN.LT.O.AND.EFDIFF.GT.O).OR.(SIGN.GT.O.AND.
18500
               C EFDIFF.LT.O)) 381.372
18600
         381
                  F2=1
18700
                  SIGN=EFDIFF
18800
                  INC =O. 1 "INC
18900
         372
                  IF (ABS(EFDIFF).LT.(EG*1E-4)) 400,385
19000
         385
                  EF=EF+(INC*F2)
19100
         390
                  CONTINUE
19200
                  WRITE(5,395) I, EFDIFF, EG, EF, NC, PT1, PT2, PT3, NB(I-1), DCDV
19300
         395
                  FORMAT(1X, EF ROUTINE UNABLE TO CONVERGE IN 50 ITERATIONS.
                  ',/,1X, QUIT AT POINT: ', I3,2X, EFDIFF=',E11.3,2X, EG=',E11.3,

EF=',E11.3,' NC=',E11.3,' PT1=',E11.3,' PT2=',E11.3,

PT3=',E11.3,' NB(I-1)=',E11.3,' DCD=',E11.3)
19400
19500
               C
19600
19700
                  PRINT 395, I, EFDIFF, EG, EF, NC, PT1, PT2, PT3, NB(I-1), DCDV
19800
         400
                  IF (I.EQ.2) DELPHI=0.01
                  DO 450 0=1,50
19900
20000
                  VB(I-1)=DELPHI+DPHIBN-(EG-EF)-VDELC(I-1)-TEMP*8.6171E-5
20100
                   IF (I.EQ.2) 410.420
20200
         410
                  W(I-1)=SQRT(ER+5.527E5+VB(I-1)/NB(I-1))
20300
                  GO TO 440
                  TERM = (SQRT(W(I-2)^{++}2+4.0^{+}5.527E5^{+}ER^{+}(VB(I-1)-VB(I-2))
20400
         420
20500
                  /NB(I-1))/2.0)
                  W(I-1)=W(I-2)/2+TERM
20600
                  IF (W(I-1).GE.O) 440,430
20700
                  W(I-1)=W(I-2)/2-TERM
20800
         430
20900
         440
                  IF (ABS(W(I-1)-WOLD).LT.0.0001E-5) GO TO 460
21000
                  WOLD=W(I-1)
21100
                   ACCDPT = (W(I-1)-W(I-2))*NB(I-1)*ACCDP
                   DELPHI=4.325E-8*SQRT(ACCDPT)
21200
21300
         C
                  WRITE (5,441) W(I-1), VB(I-1), TERM, ACCOPT, DELPHI, VDELC(I-1)
21400
         C
                  PRINT 441, W(I-1), VB(I-1), TERM, ACCOPT, DELPHI, VDELC(I-1)
                  FORMAT( W(I-1)= ,E12.4, VB(I-1)= ,E12.4, TERM= ,E12.4, ACCOPT= ,E12.4, DELPHI= ,E12.4, VDELC(I-1)= ,E12.4)
21500
         C
21600
21700
                   CONTINUE
          450
21300
                   ACCDP=ACCDPT
          460
21900
                   IF (I.EQ.2.OR.I.EQ.CPTS+1) 470,480
```

O. Management

C

```
22000
        470
                DELC(I-1)=(DELCT(I)-DELCT(I-1))/(VDELC(I)-VDELC(I-1))
22100
                 GO TO 490
                DELC(I-1)=(((DELCT(I)-DELCT(I-1))/(VDELC(I)-VDELC(I-1)
22200
        480
22300
                ))+((DELCT(I-1)-DELCT(I-2))/(VDELC(I-1)-VDELC(I-2))))/2
22400
        490
                 MT(I-1)=ABS(1.809E-6*NB(I-1)*NB(0)*W(I-1)**2*DELC(I-1)/ER)
22500
                 IF (F.NE. 1. AND. F1. NE. 1) X=0
22600
                 IF (F.NE. 1. AND. F1. EQ. 1) X=1
22700
                 IF (F.EQ.1.AND.F1.NE.1) X=2
22800
                 IF (F.EQ.1.AND.F1.EQ.1) X=3
22900
                 EGEF-EG-EF
23000
                 WRITE (5,500) X, VDELC(I-1), CCV(J), EGEF, DELPHI, DELC(I-1),
23100
               W(I-1), NB(I-1), NT(I-1)
        500
23200
                 FORMAT(2X, I1, 2X, F7.3, 7(5X, 1PE12.5))
23300
                 PRINT 500, X, VDELC(I-1), CCV(J), EGEF, DELPHI, DELC(I-1),
               W(I-1), NB(I-1), NT(I-1)
23400
23500
        510
                 CONTINUE
23600
                 PRINT 511, AREA
23700
                 FORMAT(///,1X, DEVICE AREA=",1PE12.5, CM**2")
        511
23800
                 PRINT 512, ER
23900
                 FORMAT(1X, RELATIVE DIELECTRIC CONST. = ', F6.2)
        512
24000
                 PRINT 513, DPHIBN
                 FORMAT(1X, DELA PHI B-N=", F6.2, (VOLTS)")
24100
        513
24200
                 PRINT 514, MDEE, MDEH
24300
        514
                 FORMAT(1X, DENSITY OF STATES EFFECTIVE MASS FOR ELECTRONS=',
24400
              C F4.2, AND OF HOLES= ,F4.2)
24500
                 PRINT 515, EDON
24600
        515
                 FORMAT(1X, DONOR ACTIVATION ENERGY= ,F5.3, (EV) )
24700
                 PRINT 516, TEMP
24800
                 FORMAT(1X, TEMPERATURE OF PEAK= .F6.2, (DEG K) )
        516
24900
                 PRINT 517, VBIAS
25000
                 FORMAT(1X, DC REVERSE BIAS= ,F7.2, (VOLTS) )
        517
25100
                 PRINT 520
                 FORMAT(/, FLAG CODES: O - NO DIFFICULTY; 1 - COULD
25200
        520
25300
                NOT MATCH A C(V) DATA POINT TO THIS VALUE OF VREV;
25400
                2 - DELTA C/DELTA V CRITEIA NOT MET; 7,7 3 - BOTH
25500
                  CONDITIONS 1 & 2 APPLY. ,///, 30X, CAPACITANCE DATA
                USED ABOVE ,/,6X, V-REV ,8X, HEIGHT ,9X, SENSITIVITY ,
25600
                 5X, CONVER. FACT. ,8X, DELC/C, /,5X, (VOLTS, 9X,
25700
25800
                 (CM),11X,(VOLTS),11X,(V/PF),11X,(PF/V))
25900
                 DO 540 M=1,CPTS
26000
                 PRINT 530, VDELC(M), DISP(M), S(M), CVF(M), DELCT(M)
26100
        530
                 FORMAT(5X, F7.3, 5(5X, 1PE12.5))
26200
        540
                 CONTINUE
26300
                 PRINT 545
                 FORMAT(/////)
26400
        545
                 WRITE(5,550)
26500
                 FORMAT(1X. IS THERE ANOTHER TRAP PEAK FOR THIS DEVICE? ./.
26600
        550
                1X, 1=YES, O=NO',/)
26700
                 READ(5,50) N
26800
26900
                 IF (N.EQ.1) GO TO 140
27000
                 WRITE(5,560)
                 FORMAT(1X, DO YOU WISH TO ANALYSE ANOTHER DEVICE? ,/,
27100
        560
27200
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